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初審
再審 (訴願)引証附件

(54)名稱：將諸如曼徹斯特或類似編碼數據之雜訊及斷續數據解碼之方法及裝置

(21)申請案號：85114730

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(74)代理人：蔡中曾 先生

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[57] 申請專利範圍：

1. 一種供解碼曼徹斯特編碼數據流之裝置，包含：
一過渡檢測器，供接收曼徹斯特編碼數據流，以在檢測到曼徹斯特編碼數據流之過渡時產生過渡指示輸出；
一電路，在過渡指示輸出產生後之預定時間產生輸出控制脈衝；
一取樣觸發器，接收曼徹斯特編碼數據流，受輸出控制脈衝所控制，以在輸出控制脈衝產生時輸出曼徹斯特編碼數據之狀態。
2. 根據申請專利範圍第1項之裝置，其中上述取樣觸發器操作，以產生二進制NRZ形式之曼徹斯特編碼數據流。
3. 根據申請專利範圍第1項之裝置，另包含一時鐘發生器，供在頻率高於曼徹斯特編碼數據流產生一時鐘脈衝流。
4. 根據申請專利範圍第3項之裝置，其中上述過渡檢測器連接為接收時鐘脈衝流，並構形為使過渡指示輸出與時鐘脈衝流之脈衝同步。
5. 根據申請專利範圍第1項之裝置，另包含一選相器，以選擇在過渡後所出現之曼徹斯特數據單元之已知一半。
6. 根據申請專利範圍第5項之裝置，其中上述選相器選擇曼徹斯特數據單元之第二一半。
7. 根據申請專利範圍第5項之裝置，其中上述選相器選擇性曼徹斯特數據單元之第一一半。
8. 根據申請專利範圍第7項之裝置，另包含一使來自觸發器之輸出反相之反相器。
9. 一種定時回復及曼徹斯特數據解碼系統，包含：
一振盪器，提供輸出脈衝；
一多模式輸入電路，連接為接收可包含曼徹斯特編碼數據信號之輸入信號，並輸出一包含信號之數據；
一過渡檢測器，連接為接收來自多模

公告本

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（以上各欄由本局填註）

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發明 ~~新型~~ 專利說明書

一、發明 ~~新型~~ 名稱	中文	將諸如曼徹斯特或類似編碼數據之雜訊及斷續數據解碼之方法及裝置
	英文	METHOD AND APPARATUS FOR DECODING NOISY, INTERMITTENT DATA, SYCH AS MANCHESTER ENCODED DATA OR THE LIKE
二、發明 ~~創作~~ 人	姓名	郝威廉 (William A. White)
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	國籍	美國籍
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	代表人姓名	郝威廉(William E. Hiller)

裝 訂 線

331680

（由本局填寫）

承辦人代碼：	
大　　類：	
ＩＰＣ分類：	

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本案已向：

美　　國（地區）　申請專利，申請日期：西元1995年11月13日　案號：60/006,617,　□有　☒無主張優先權

有關微生物已寄存於：　　，寄存日期：　　，寄存號碼：

（請先閱讀背面之注意事項再填寫本頁各欄）

裝　訂　線

五、發明說明（ 1 ）

發明之背景

1.發明之領域

本發明係關於將諸如曼徹斯特或類似編碼數據之雜訊，斷續數據，解碼之方法及裝置之改進，並另係關於依所接收之數據信號而定，具有多重操作模式之方法及電路。

2.相關背景

曼徹斯特編碼數據可用於供可靠傳輸遙測及其他型式之數據。通常，在此項技藝上已知，例如曼徹斯特編碼數據流可自編碼遙測數據流產生，其可例如爲一種二進制不歸零(BNRZ)編碼信號（或藉另一相似技術編碼之數據流）。在接收曼徹斯特編碼信號時，信號予以解碼，以回復原始BNRZ編碼信號。藉任何裝置，特別是經由射頻傳輸在數據傳輸所固有之諸多問題之一，爲信號變爲雜訊，積聚靜電，或其他射頻信號或雜訊。這使解碼曼徹斯特信號難以可靠進行。

廣爲用於數據傳輸及遙測方面之曼徹斯特編碼，藉在編碼信號之中點過渡之方向，界定予以編碼之信號之數據狀態，其將變爲曼徹斯特編碼數據流。曼徹斯特編碼數據流具有相等持續時間之時間順序"單元"。在每一單元之中點，數據在指示予以編碼之信號狀態之方向改變狀態。

因此，例如，指示予以編碼之信號之高至低邏輯狀態過渡，爲在邏輯低狀態。在另一方面，指示予以編碼之信號之低至高邏輯狀態過渡，爲在邏輯高狀態。當然，在每一單元之端點，將會形成曼徹斯特編碼數據流之信號狀態必

五、發明說明（ 2 ）

須置定或建立，以啓動次一中點過渡。因此，如果邏輯零予以編碼，將會形成曼徹斯特編碼數據流之信號必須在初始邏輯高狀態，以便可完成高至低之中點過渡。要不然，如果邏輯一予以編碼，將會形成曼徹斯特編碼數據流之信號必須在初始邏輯低狀態，以便可完成低至高之中點過渡。

因此可看出，如果一系列相同之邏輯狀態予以編碼，所產生之曼徹斯特編碼信號將爲一週期等於單元長度之方波。在另一方面，如果一系列交替邏輯一及零予以編碼，所產生之曼徹斯特編碼信號將爲一週期等於二倍單元長度之方波。

人們曾建議不同之方法供解碼曼徹斯特編碼數據。一受人歡迎之技術爲使用一種鎖相回路。但在實際上，有時候曼徹斯特編碼信號予以格式化爲提供一種"叫醒"順序，諸如十數據單元，後隨一短停滯時間，後隨實際之數據。由於叫醒順序很短，僅10數據單元，而致電路可能不鎖定並可能在短停滯時間漂移。因此，常用之鎖相回路解碼技術無法使用。其他解碼技術採用類比及數位匹配之濾波器，整合及轉儲方案，以及高度過取樣數位信號處理技術。長同步時間及高組份計數排除使用大多數此等方案。

人們曾建議一種方法，採用一種選通電路，其響應在曼徹斯特編碼波形之中間單元過渡，以產生一啓動信號。啓動信號導使時鐘電路產生高頻率時鐘脈衝，其積聚在一可程式計數器。如果計數器超過在後隨啓動信號開始前之時

五、發明說明（ 3 ）

鐘計數界限，便導使一儲存元件取樣及儲存編碼波形。

發明之概述

由於以上情形，因此，本發明之目的爲提供一種供曼徹斯特數據解碼及定時回復之改進電路及方法。

本發明之另一目的爲提供一種所說明型式之改進電路及方法，其依輸入信號之性質而定，具有不同操作模式。

本發明之另一目的爲提供一種所說明型式之改進電路及方法，其有一"叫醒"操作模式，在此模式無輸出產生，直到收到預定順序曼徹斯特數據。

本發明之另一目的爲提供一種所說明型式之改進電路及方法，其有一"保持"模式，在此模式可能出現無曼徹斯特數據收到之預定停滯時間週期，並且在其期間保持電路之偏壓。

精於此項技藝者自本發明之下列詳細說明，配合附圖及後附之申請專利範圍，將會明白本發明之此等及其他諸多目的，特色以及優點。

根據本發明之一廣義方面，提供一種供解碼曼徹斯特編碼數據流之裝置。該裝置包括一過渡檢測器，供接收曼徹斯特編碼數據流，以產生過渡：指示在檢測到曼徹斯特編碼數據流過渡時之輸出。也提供一電路，以在過渡指示輸出產生後一段預定時間產生輸出控制脈衝。一取樣觸發器接收曼徹斯特編碼數據流，並受輸出控制脈衝所控制，以在輸出控制脈衝產生時輸出曼徹斯特編碼數據狀態。

在一種較佳實施例，取樣觸發器操作，以產生一種二進

五、發明說明（ 4 ）

制NRZ形式曼徹斯特編碼數據流。過渡檢測器可構形爲使過渡指示輸出與時鐘脈衝流之脈衝同步，並且也可包括一選相器，以選擇曼徹斯特數據之第一或第二符號，供鎖存及自裝置輸出。

根據本發明之另一廣義方面，提供一種叫醒電路供響應在輸入信號之曼徹斯特數據叫醒順序，自靜止狀態開始曼徹斯特編碼數據檢測器之操作。電路包括一低通濾波器電路及在最初斷開之保持電路，以在曼徹斯特編碼數據檢測器在靜止狀態時接收輸入信號。低通濾波器電路產生一對應於輸入信號平均值之輸出信號。一在最初爲導通之補償電路使低通濾波器輸出信號偏移，以產生一參考電壓。一比較器電路產生一對應於參考電壓與輸入信號間之差異之

（請先閱讀背面之注意事項再填寫本頁）

五、發明說明（ 5 ）

補償電路也可包括一第一電阻器，連接於微分放大器之反相輸入與一參考電壓之間，第二電阻器連接於非反相輸入與輸入信號之間。一開關可連接爲與第一電阻器串聯，以將補償電路接通，因而在反相輸入之電壓對應於輸入信號平均值加一補償電壓。在第一開關接通時，微分放大器之輸出產生數據輸出信號對應於輸入信號脈衝補償電壓平均值與輸入信號間之差異。

比較器電路也可包括與第一電阻器串聯之第二開關，因而在第二開關接通並且第一開關斷開時，微分放大器之輸出產生輸入信號與輸入信號平均值間之放大差異。

根據本發明之又一廣義方面，提供一種方法，供解碼曼徹斯特編碼數據，以產生數據之一種不歸零二進制表示法。該方法包括產生一脈衝供曼徹斯特編碼數據之每一過渡，並產生一在定時相位之取樣信號，有脈衝供曼徹斯特編碼數據之每一過渡。曼徹斯特編碼數據然後在每次出現取樣信號時予以鎖存，並產生鎖存數據之輸出。一自適應界限檢測用以接收曼徹斯特編碼數據，而具有增強之雜訊免受性。在一種實施例，使用自適應界限檢測之步驟包括在一解碼電路之數據輸入級提供許多操作模式，諸如一"穩態"模式及"補償"操作模式。在一種實施例，提供一種"叫醒"操作模式。

根據本發明之又一廣義方面，提供一種定時回復及曼徹斯特數據解碼系統。該系統包括一振盪器，提供輸出脈衝及一多模式輸入電路連接爲接收一可包含曼徹斯特編碼數

五、發明說明（ 6 ）

據信號之輸入信號，並輸出一包含信號之數據。一過渡檢測器連接爲接收來自多模式輸入電路之輸出信號，供產生一曼徹斯特過渡指示在所有曼徹斯特數據過渡之脈衝。一藉曼徹斯特過渡電路所同步之計數器連接爲將來自振盪器之輸出脈衝除以一預定計數，以產生輸出脈衝，在曼徹斯特數據過渡後開始預定數之振盪器脈衝。一除2 電路予以連接爲接收來自計數器電路之脈衝，以產生一樣本命令信號，並且一取樣電路連接爲接收來自除2 電路之輸出及曼徹斯特編碼數據，以響應來自除2 電路之輸出鎖存曼徹斯特編碼數據狀態。

在一種實施例，定時回復及曼徹斯特數據解碼系統也可包括一模式解碼器電路，其可爲一邏輯閘陣列或相似電路，連接爲接收來自計數器電路之輸出計數，以在來自計數器電路之輸出計數之預選計數提供輸出。一模式控制電路也可連接爲接收模式解碼器電路之至少有些輸出，模式控制電路予以連接爲選擇性控制多模式輸入電路之模式。

定時回復及曼徹斯特數據解碼系統也可包括輸出控制電路，連接爲接收取樣電路所鎖存之數據及指示脈衝之過渡，供產生一NRZ輸出數據信號並輸出定時脈衝，並且，如果希望，一電路延遲輸出定時脈衝振盪器頻率之一半週期。

多模式輸入電路在一種實施例有一種"穩態"模式，在此模式，一包含曼徹斯特編碼數據流之信號予以處理，並在輸出產生一輸出二進制NRZ信號，一"補償"模式，在此模式，需要出現叫醒曼徹斯特數據順序導使電路"叫醒"，以

五、發明說明（ 7 ）

採取並恢復"穩態"操作模式，及一"保持"模式，在此模式，即使不接收"穩態"模式曼徹斯特編碼數據也保持電路偏壓。

多模式輸入電路可包括一有反相及非反相輸入之比較器，有一第一電阻器，輸入信號藉其予以連接至非反相輸入，及一第二電阻器，輸入信號藉其加至反相輸入。一第三電阻器在一端連接至比較器之反相輸入。一第一開關功能與第二電阻器串聯連接，及一第二開關功能連接於第三電阻器之另一端與一參考電壓之間。一第一電容器連接於比較器之反相輸入與接地之間，及一第二電容器連接於非反相比較器之輸入與接地之間。第一及第二開關功能受模式控制電路所控制。

根據本發明之又一廣義方面，提供一種裝置供在曼徹斯特數據流產生一對應於曼徹斯特單元第二半狀態之NRZ數據信號。該裝置包括一振盪器，以產生一時鐘脈衝流，及一脈衝發生器連接爲接收曼徹斯特數據流，供在曼徹斯特數據流在每一過渡產生輸出脈衝。一除n 計數器連接爲藉來自振盪器之時鐘脈衝予以計時，並藉來自脈衝發生器之脈衝予以重設，除n 計數器具有在預定數之時鐘脈衝後改變狀態之輸出。一定時觸發器連接爲藉來自除n 計數器之輸出予以計時，觸發器予以連接爲在來自除n 計數器之輸出之所有第二計數產生一輸出。一取樣觸發器予以連接爲在數據輸入接收曼徹斯特數據流，及在時鐘輸入接收定時[illegible]

（請先閱讀背面之注意事項再填寫本頁）

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五、發明說明（ 8 ）

供其時曼徹斯特數據流在輸出之現存狀態。一順序計數器予以連接爲在時鐘輸入接收除n 計數器之輸出，及在重設輸入接收來自脈衝發生器之輸出脈衝，從而順序計數器產生一指示在二倍寬曼徹斯特脈衝已出現時之信號，信號予以連接爲重設定時觸發器。

根據本發明之又一廣義方面，提供一種方法，供在曼徹斯特數據流產生一NRZ數據信號對應於每一曼徹斯特單元之已知一半之狀態。該方法包括在曼徹斯特數據流之每一過渡產生一過渡脈衝，及在曼徹斯特數據流產生一系列定時脈衝具有曼徹斯特單元頻率n 倍之頻率之步驟。系列定時脈衝響應每一過渡脈衝而重新開始，並在出現每一第m 定時脈衝時，鎖存曼徹斯特單元之目前狀態，其中m 大於n/2。定時脈衝同時計數爲提供一定時脈衝計數，計數響應每一過渡脈衝予以重新開始。如果定時脈衝計數變爲大於n/2，便進行鎖存，以在次一第(n/2)出現定時脈衝時鎖存曼徹斯特數據流。

在本發明之又一廣義方面，提供一種方法，供在曼徹斯特數據流產生一對應於曼徹斯特單元之第二半狀態之NRZ數據信號，其中在曼徹斯特數據流產生一系列定時脈衝有一二倍曼徹斯特單元頻率之頻率。在出現每一第二定時脈衝時，鎖存曼徹斯特單元之目前之狀態。檢測在曼徹斯特數據流出現二倍寬脈衝，並使鎖存重新同步，以在已檢測到二倍寬脈衝後在其次出現之定時脈衝開始。

附圖之簡要說明

五、發明說明（ 9 ）

附圖中例示本發明，在附圖中：

圖 1 示一代表性曼徹斯特數據流，以及使用根據本發明較佳實施例之定時回復及解碼系統，自其所獲得之不歸零數據流。

圖 2 爲一根據本發明之較佳實施例，供解碼曼徹斯特數據之通常系統之電方塊圖，配合圖 3 中所示之不同波形，例示系統之總體操作，及供使系統同步以檢測每一曼徹斯特數據單元之預定一半之機構。

圖 3 示在操作圖 2 之電路時所產生之一系列波形，示系統藉以自動識別存在有效曼徹斯特數據，以及系統藉以將其解碼之方式。

圖 4 爲一根據本發明，與圖 2 者相似，供解碼曼徹斯特數據之系統之電方塊圖，具有另外之短及長停滯時間檢測特色，並具有長期睡眠及叫醒能力。

圖 5 爲更詳細之電示意方塊圖，示一根據本發明之較佳實施例，供曼徹斯特或類似編碼數據之定時回復及解碼系統。

圖 6 爲一供用於圖 5 之定時回復及解碼系統之振盪器之電示意圖。

圖 7 爲一供用於圖 5 之定時回復及解碼系統之過渡檢測器之電示意圖。

圖 8 爲一供用於圖 5 之定時回復及解碼系統之過渡計數器之電示意圖。

圖 9 爲一供用於圖 5 之定時回復及解碼系統之除二電路

五、發明說明（10）

之電示意圖。

圖10爲一供用於圖5之定時回復及解碼系統之模式解碼器電路之電示意圖。

圖11爲一供用於圖5之定時回復及解碼系統之脈衝發生器電路之電示意圖。

圖12爲一供用於圖5之定時回復及解碼系統之模式控制電路之電示意圖。

圖13爲一供用於圖5之定時回復及解碼系統之過渡計數器電路之電示意圖。

圖14爲供用於圖5之定時回復及解碼系統，供傳送NRZ數據輸出及已自包含曼徹斯特編碼數據之輸入數據流所獲得之附帶定時或觸發器脈衝之輸出電路之電示意圖。

圖15爲一供用於圖5之定時回復及解碼系統之測試模式選擇電路之電示意圖。

圖16a-c爲例證性電波形，示在圖5之定時回復及解碼系統之每一操作模式，來自圖15之界限檢測器電路之輸出信號。

圖17示一與一可用於本發明之電路之叫醒順序及短停滯時間間隔之串聯之波形脈衝。

圖18爲根據本發明之一方面，在輸入比較器電路之不同節點，在叫醒順序時之一系列詳細波形。

圖19爲一供用於圖1之定時回復及解碼系統界限檢測器電路之更詳細電示意圖。

在不同之諸圖中，相同參考數字用以標示相同或相似部

五、發明說明（ 11）

份。

較佳實施例之詳細說明

圖1示一曼徹斯特編碼數據之實例。波形10有一順序之相等長度數據單元12-22，每一單元表示對應二進制數據之一位元。在所有單元之中點有過渡，其將曼徹斯特數據單元分爲二間隔或符號。正變爲中間單元過渡，諸如過渡25表示二進制1；負變中間單元過渡，諸如過渡26表示二進制0。

固定系列之0 或固定系列之1 產生完全相同方波，具有脈衝寬度等於一符號時間及週期等於一單元時間，諸如單元12-15或單元20-22。波形僅在相位有所不同。其無其他資訊，諸如，二相鄰符號是否在相同單元或在相鄰單元，或同樣，是否過渡在中間單元或在單元邊界，便無法加以區別。

對照於固定1 或固定0，交替1 及0 之曼徹斯特表示法不含糊不清。"10" 產生一二符號寬度曼徹斯特高，諸如單元16及17所表示，以及"01"產生二符號寬度曼徹斯特低，諸如單元17及18所表示。此等二倍寬脈衝始終跨在單元邊界上，並因此提供一基礎，供使用於實施本發明電路實施例之定時參考定向。一旦定時參考建立，單一寬度脈衝表示固定數據可正確解碼。

圖2中示供解碼曼徹斯特數據之系統400之概括電方塊圖，其中配合圖3中所示之不同波形，例示總體系統之操作。一振盪器35提供系統之定時，其產生一時鐘脈衝流，

五、發明說明（ 12）

如在圖 3 中所見爲標明"SCLK"。曼徹斯特數據流予以解碼，標示MDAT，使在輸入線路88進入系統400，標示DOUT之解碼數據在線路255自系統輸出，並且，標示TRIG之解碼定時，在線路259輸出。

曼徹斯特數據最初連接至過渡觸發單觸發脈衝發生器45（在本案稱作過渡檢測器45）之輸入，其在每一正或負變數據過渡產生一單一輸出脈衝，輸出脈衝在線路83標示M2DAT。圖 3 中示MDAT及M2DAT之代表性波形。自圖 3 可看出，MDAT不必要與來自振盪器35之時鐘脈衝SCLK同步，但在MDAT之每一過渡存在一M2DAT脈衝。

在線路83來自過渡檢測器45之M2DAT輸出信號連接爲清除或重設一除5 計數器75，其連接爲在線路87藉來自振盪器35之時鐘脈衝SCLK予以計時。除5 計數器75具有不同之單獨輸出供每一計數，供計數3 之輸出（在本案稱作"計數-3輸出"）連接爲對一D-型觸發器105計時，並且供計數 4 之輸出予以接回至重設過渡檢測器45。來自除5 計數器75之輸出爲一標明2XCK之波形，有一頻率爲二倍曼徹斯特數據信號MDAT之預期頻率。

在正常操作，D-型觸發器105在2XCK信號之每一第二過渡對取樣D-型觸發器120計時，對應於所檢測曼徹斯特單元之第二半。由於除2D-型觸發器105之輸出連接爲對取樣D-型觸發器120計時，每當來自D-型觸發器105之信號SSMS改變狀態自負至正，取樣D-型觸發器120對其時在線路88存在之曼徹斯特數據至在線路255之輸出DOUT之狀態計時

五、發明說明（ 13）

。取樣D-型觸發器120因此在線路255產生一NRZ數據輸出DOUT，複製來自D-型觸發器120予以計時之每一連續時間之曼徹斯特數據之狀態。

請予察知，如果不採取適當同步預防措施，系統將可能鎖定至2XCK脈衝之一數據解碼順序，對應於曼徹斯特數據單元第一半之定時。因此，來自除5 計數器之計數-3輸出也連接爲對一順序計數器402計時。順序計數器402操作，以在線路83藉M2DAT信號予以重設前，計數2XCK信號之預定數過渡。例如，在例示之實施例，2XCK信號之二過渡在順序計數器402之計數-2輸出予以計數，產生一種狀態改變。因此，來自順序計數器402之計數-2輸出之輸出在線路107提供一信號DB2INI，其指示在曼徹斯特數據出現二倍寬脈衝，並用以重設除2D-型觸發器105。

如所述及，在例示之實施例，第二半曼徹斯特單元希望予以取樣。因之，在MDAT脈衝之單一狀態檢測何時出現二連續2XCK脈衝(亦即，預期中點過渡但未出現之一種狀態)，藉以開如定向過程。更特別爲，請參照圖3，每當二連續2XCK脈衝出現而無中間曼徹斯特數據狀態改變，指示一"二倍寬"曼徹斯特數據脈衝已出現，諸如脈衝404或脈衝426，輸出DB2INI在線路107改變狀態，以清除D-型觸發器105，以使系統與每一曼徹斯特數據單元之第二半同步。

例如，圖示之第一MDAT脈衝404爲一"二倍寬"脈衝，係例如，由予以解碼之曼徹斯特信號所表示數據之"01"或"10"值所產生。二倍寬脈衝在其個別正及負變過渡在M2DAT

五、發明說明（ 14）

信號產生過渡406及407。第一M2DAT脈衝406重設除5 計數器，其繼續進行，以對時鐘脈衝SCLK計數。其也重設順序計數器402。在計數-3輸出之輸出2XCK保持低，如信號區段410所示，直到三時鐘脈衝已出現，計數-3輸出在其時予以設定。計數-3輸出保持高，供脈衝區段411所示之二另外計數，直到除5 計數器達到計數5。

在此時間，由於無狀態改變出現在曼徹斯特數據脈衝404，無過渡檢測脈衝在M2DAT流產生，故除5 計數器繼續進行，以立即計數新數據順序。在第二計數3 後，除5 計數器之輸出改變狀態，2XCK數據流區段414及416所示。另外，由於順序計數器402不予重設，由於沒有MDAT過渡，故在第二連續2XCK脈衝416出現時，產生一同步脈衝DB2INI。可看出在二倍寬曼徹斯特脈衝後，其次出現之狀態改變將爲一適當中點過渡。因此，在DB2INI脈衝重設除2D-型觸發器105時，在下次出現之2XCK信號出現時，除2D-型觸發器105產生一SSMS信號，保證爲在曼徹斯特單元之第二半，以對取樣D-型觸發器120計時，從而使系統同步，以對隨後出現之曼徹斯特數據單元之第二半取樣。

再更特別爲，如圖所示，在曼徹斯特數據脈衝區段404後，曼徹斯特數據信號在2XCK信號之區段418中，在次一計數3 SCLK脈衝前經歷中點過渡至區段426。這導使產生一指示M2DAT脈衝407之過渡，其重設除5 計數器並開始一新計數。其次出現之2XCK脈衝419，其出現在曼徹斯特數據單元定時之第二半，對D-型觸發器105計時，其復對取

五、發明說明（15）

樣D-型觸發器120計時，其取樣並鎖存在該時間存在之曼徹斯特數據。

請予察知，雖然定時2XCK脈衝已說明爲曼徹斯特數據單元者之二倍，但可配合對除法器之適當調整，選用任何多倍n，以選擇在每一曼徹斯特單元之第二半出現之特定2XCK脈衝。藉順序計數器所提供之重設調整也可改變，以重設輸出鎖存，以選擇藉以啓動鎖存功能之適當數之脈衝例如n/2。

在輸出線路255產生數據之同時，在輸出線路257產生在線路87與時鐘脈衝SCLK同步，標明TRIG之觸發器脈衝。在圖3中可看出每一TRIG脈衝與脈衝SSMS升緣之關係。

現請參照圖4，圖示一供解碼曼徹斯特數據之系統430之電方塊圖，其與以上參照圖2所說明者相似。圖4中所示之系統430具有短停滯時間暫存器431及長時間暫存器432所提供之另外短及長停滯時間檢測特色以及長期睡眠及叫醒能力。短及長停滯時間暫存器用以調整輸入曼徹斯特數據調節電路41之界限，並在未檢測到曼徹斯特數據預定時間長度時中止系統430之輸出。以下詳細說明系統430之短及長停滯時間特色之操作。

另外，圖4之系統430包括一種由長停滯時間暫存器及一單獨之叫醒計數器165所提供之睡眠及叫醒特色。以下也詳細說明睡眠及叫醒特色之操作。

現請參照圖5，示一根據本發明較佳實施例之定時回復及曼徹斯特數據解碼系統34之更詳細方塊圖。50 kHz自由

五、發明說明（16）

運作振盪器35對電路之其餘部份提供基本定時參考。振盪器35可爲標準構造，圖6中示其一實施例之細節。雖然圖示振盪器35由分立邏輯組份，諸如圖示之交叉耦合"反及"閘39所構成，但振盪器功能可由熟知之裝置，或其他適當振盪器裝置或電路(未示)提供。

請再次參照圖5，可包含予以解碼之曼徹斯特數據編碼數據流之輸入信號，在輸入線路40連接至多模式輸入電路41，其在線路42提供其輸出(MDAT)至過渡檢測器45。（在例示之實施例，提供以下所詳細說明之測試模式控制電路55，其控制輸入信號抑或測試信號加至定時回復及曼徹斯特數據解碼系統34之其餘部份。來自測試模式控制電路55之輸出然後傳送至過渡檢測器45。）

多模式輸入電路41有一比較器46，具有如圖所示之反相及非反相輸入。輸入信號藉第一電阻器47連接至非反相輸入，並藉第二電阻器48連接至反相輸入。一與電阻器48串聯連接之第一開關50受以下所詳細說明之模式控制電路160所控制。雖然一實體開關，或一連接成已知開關功能構形之電晶體可提供第一開關50，但請察知，目的爲選擇性施加輸入信號至比較器46之反相輸入。因之，等效電路可用以進行此選擇性電壓施加，其一實例爲例如在圖19中所示多模式輸入電路41之一種實施所示之轉運閘283。

一第三電阻器56連接於比較器46之反相輸入與第二開關58之間，其也受模式控制電路160所控制。開關58連接至一參考電壓，諸如圖示之Vcc。而且，一實體開關，或一

五、發明說明（ 17）

連接成已知開關功能構形之電晶體可提供第二開關58；但請察知，目的爲將電壓Vcc選擇性連接至比較器46之反相輸入。因之，等效電路可用以進行此選擇性電壓施加，其一實例爲例如在圖19中所示多模式輸入電路41之一種實施所示之電流源280及鏡電路281。二電容器60及61分別連接於比較器46之反相與非反相輸入之間，以及非反相輸入與接地之間。

產生正曼徹斯特過渡指示脈衝(M2DAT)之過渡檢測器45，在曼徹斯特數據所有過渡，正或負，在線路42接收在圖7中所示D-型觸發器64之輸入來自多模式輸入電路41之輸出。在線路87來自振盪器35之時鐘脈衝對D-型觸發器64計時，其輸出予以連接至"互斥或"閘65之輸入。"互斥或"閘65之輸出予以連接至"反及"閘66之輸入，其輸出予以連接至包括"反及"閘68及69之觸發器67之輸入。

觸發器67之另一輸入接收在線路71來自以下所詳細說明之計數器75信號，以保證過渡檢測器45不響應二過渡之第二過渡，其分開一時間少於預定數之時鐘脈衝，例如，少於約60至80微秒。觸發器67之輸出經由反相器77及78以及電阻器79連接至"反及"閘66之第二輸入。一電容器81連接於反相器78之輸入與接地之間，以配合電阻器79提供一低通濾波器。

來自"反及"閘66之輸出予以連接至一反相器84，每當正或負過渡出現在輸入線路42，其操作以在輸出線路83產生一例如約12毫微秒長之正脈衝(M2DAT)。一反相輸出出現

五、發明說明（ 18）

在線路85，標明"M2DATZ"。以下所說明之曼徹斯特過渡計數器75可選定第一或第二曼徹斯特符號，其由振盪器35予以計時，並如曼徹斯特過渡指示脈衝(M2DAT)所指示，在在線路85a出現曼徹斯特數據過渡時重設。

圖5中示適當曼徹斯特過渡計數器電路75之細節，其中在輸入線路87收到來自振盪器35之時鐘脈衝，並在輸入線路85收到來自過渡檢測器電路45之輸出。曼徹斯特過渡計數器75有三D-型觸發器90，91，及92連接爲在線路87在其個別時鐘輸入接收時鐘脈衝，並在其清除或重設輸入，接收曼徹斯特過渡信號。來自第一D-型觸發器90之輸出予以連接至第二D-型觸發器91之數據輸入，並且第二及第三D-型觸發器91及92之輸出藉"反或"閘94連接至第一D-型觸發器90之輸入。另外，第二及第三D-型觸發器91及92之輸出藉反相器98連接至"反及"閘96之輸入，第二D-型觸發器91之輸出予以反相。

在計數器35已藉在線路85出現曼徹斯特數據過渡予以重設後，曼徹斯特過渡計數器75操作如模數5 時鐘脈衝計數器，在振盪器35在線路87產生三計數後，有已除時鐘脈衝在輸出線路100出現。如果無曼徹斯特數據過渡重設事件出現，在輸出線路100之已除時鐘脈衝僅爲時鐘頻率除以五。在曼徹斯特數據過渡重設事件出現在線路85後，信號在輸出線路71在所有四計數後出現，並予以接回至以上所說明之過渡檢測器45之觸發器68之輸入。

請予察知，本案所說明之本發明之特定電路實施例，曼

五、發明說明（ 19）

徵斯特過渡計數器75所產生之延遲計數所確定，取樣並鎖存每一旻徵斯特數據單元之第二符號，藉以將旻徵斯特數據解碼。請予察知，旻徵斯特數據之第一符號也可藉選擇不同之延遲計數，然後使數據反相予以取樣，鎖存，及解碼。

在輸出線路100來自計數器75之已除時鐘脈衝予以連接至除2 電路105之輸入，圖 9 中示其細節。除2 電路105有一D-型觸發器106，其在線路100在其時鐘終端接收來自計數器75之已除時鐘脈衝。重設線路予以連接爲接收來自以下所詳細說明之模式解碼器電路110之重設信號。D-型觸發器106之輸出藉"反及"閘112予以反相，並連接至輸入。"反及"閘112之另一邊予以連接爲在線路113接收來自模式解碼器電路110之信號，其指示在線路100，已除時鐘脈衝之三連續週期已無旻徵斯特數據過渡。信號在線路113藉反相器114予以反相。

在操作時，除2 電路105在線路100將已除時鐘脈衝除以二，以在輸出線路117產生樣本命令信號。吾人將會明白，在線路100，在任何二連續旻徵斯特數據過渡之間已出現已除時鐘脈衝之二正緣，指示在線路85之脈衝時，在線路107將會產生重設信號。由於過渡必須出現在每一旻徵斯特單元之符號之間，如果在線路100之已除時鐘脈衝之二計數已出現在旻徵斯特數據過渡之間，第二計數產生一重設信號，保證使電路與旻徵斯特單元之正確符號同步，並且二倍寬脈衝已出現（例如比較圖 1 中之二倍寬脈衝27）

五、發明說明（ 20）

。二倍寬脈衝始終在線路100重疊二已除時鐘信號脈衝之前緣，而單一寬度脈衝始終僅重疊一。由於在線路107之重設信號重設D-型觸發器106，故除2 電路105之操作自動使電路同步，以在線路100出現已除時鐘脈衝之次一計數脈衝時，檢測正確曼徹斯特符號及其後每隔一者。

在D-型觸發器106已重設後，在線路100之已除時鐘脈衝之次一正緣導使在線路117之樣本命令信號變高，致動樣本方塊(以下所說明)，以取樣在第二曼徹斯特數據符號時所接收之曼徹斯特數據。如果三連續週期已除時鐘脈衝在線路100無曼徹斯特數據過渡，在線路113所傳送之信號變高，強制"反及"閘112之輸出爲高。這導使在線路100出現現已除時鐘脈衝之次一正緣時，樣本命令信號在線路117變高。曼徹斯特數據過渡再次開始時，D-型觸發器106便行設定，以取樣曼徹斯特單元之第二半，由於在線路100之已除時鐘脈衝之第一正緣將會在線路117對樣本命令信號計時至其低狀態。在線路100之已除時鐘脈衝之次一正邊緣對至高狀態之輸出計時，其導使樣本電路120對目前之曼徹斯特數據取樣。

如圖中所示5，取樣電路120在例示之實施例爲一D-型觸發器121。包含曼徹斯特數據之信號(MDAT)予以連接至數據輸入，並且輸出予以連接至以下所說明之輸出控制電路125。以每一曼徹斯特數據單元之第二符號之頻率及相位之取樣脈衝對D-型觸發器121計時，取樣觸發器121便在線路250正確取樣及鎖存曼徹斯特數據信號。在此請予察知

五、發明說明（ 21）

，由於鎖存受徵斯特數據之邏輯電平在樣本之間爲固定，所產生之數據爲圖1中波形30所示編碼數據之一種二進制不歸零(BNRZ)二進制表示法。

如以上所討論，在線路100選擇每隔一已除時鐘脈衝，藉以提供正確頻率供取樣脈衝波形。然而，不必預置，取樣脈衝同樣可能會與第一而非第二符號對準，並且解碼數據將會反相。適當對準藉模式解碼器電路110所確定，其檢測二倍寬受徵斯特波形之存在。圖10中示模式解碼器電路110之細節。

通常，模式解碼器電路110解碼來自以下所詳細說明之脈衝發生器電路130之計數，並且基本上爲一邏輯閂陣列，其在已知邏輯狀態之輸出線路132-136及107提供輸出供不同之輸入計數組合。電路有四輸入"反及"閘140-143，其在線路180-188接收來自脈衝發生器電路130之輸出。

"反及"閘140及141在線路181-185接收其來自脈衝發生器電路130之輸入。來自"反及"閘140及141之輸出連接至"反或"閘150之輸入，在線路132產生輸出，其在線路180-185之所有計數信號爲高時，在線路100在已除時鐘脈衝之計數63變高。信號在輸出線路132用以如以下所說明制止輸入至脈衝發生器電路130。

"反或"閘153接收來自"反及"閘142及143之輸出，以及在線路185之輸入，以在線路154產生一輸出，在線路100指示三已除時鐘脈衝之計數。線路154予以連接至"反及"閘155之二輸入，其作如一反相器，並連接至由"反或"閘

五、發明說明（ 22）

156及157所界定之觸發器161之輸入，以在第三計數已出現時設定觸發器。在線路133來自"反及"閘155之輸出，在線路100在三已除時鐘脈衝之計數變低，並如以下所說明，用以清除過渡計數器電路165。同時，在線路134來自觸發器之輸出，在線路100在三已除時鐘脈衝之計數變高，並如以上所說明，用以啓動除2 電路105之"反及"閘（圖 9）。

至"反或"閘156及157所構成之觸發器之另一輸入予以連接爲在線路83接收來自過渡檢測器45之信號（圖 7），指示受徵斯特數據過渡之出現。在收到信號指示受徵斯特數據過渡已出現時，觸發器予以重設，使輸出狀態在線路133回至高狀態，並使輸出狀態在線路134回至低狀態。

來自"反及"閘143之輸出，以及在線路185之信號，予以連接至"反或"閘159之輸入。來自"反或"閘159之輸出，以及在線路181之信號予以連接至"反及"閘162之輸入，在線路107產生輸出，其在線路100在二已除時鐘脈衝之計數變低。在線路107之信號用以重設圖 9 之除2 電路105之D-型觸發器106。以下所詳細說明，來自過渡計數器165之輸出信號藉一反相器167在線路166反相，並係在輸出線路136產生，以重設以下所說明之模式控制電路160之D-型觸發器135。

圖11中詳示在線路100提供已除時鐘脈衝之計數至模式解碼器電路110之脈衝發生器電路130。脈衝發生器電路130包括六D-型觸發器170-175，連接如一脈動計數器。在線

五、發明說明（ 23）

路100之已除時鐘脈衝以及指示在線路132計數已達到63之信號（圖10中所示來自模式解碼器電路110之"反及"閘150）予以加至"或"閘177之輸入。計數器藉在線路85出現曼徹斯特數據過渡指示信號予以重設，並在線路100藉已除時鐘脈衝予以計時，其藉"或"閘177予以啓動。輸出在線路180-188產生，並傳送至以上所說明之模式解碼器電路110。

脈衝發生器電路130之操作爲在線路100計數已除時鐘脈衝之數，其出現在線路85指示出現曼徹斯特數據過渡之脈衝之間。在線路85曼徹斯特數據過渡指示脈衝之出現預先設定計數器至全部"一"初始狀態，在此狀態後，已除時鐘脈衝在線路100予以順序計數。如果達到計數63，來自模式解碼器電路110之信號在線路132變高，制止進一步計時，直到次一曼徹斯特數據過渡指示脈衝出現。

模式控制電路160產生另外之控制信號，圖12中示其細節。模式控制電路160包括一D-型觸發器135連接爲在線路132接收來自圖13之模式解碼器電路110之輸出。在線路132之輸出指示已除時鐘脈衝之計數在線路100已達到63。D-型觸發器135連接爲藉在圖13之線路136來自模式解碼器電路110之輸出予以重設，其表示在以下所說明之線路166來自過渡計數器165之反相輸出。D-型觸發器135連接爲在經由"或"閘235所連接之線路100藉已除時鐘脈衝予以計時。來自D-型觸發器135之輸出予以連接至"或"閘235之第二輸入，以在輸出爲高時制止在線路100之已除時鐘脈衝。

五、發明說明（ 24）

來自D-型觸發器135之反相輸出予以連接至"反及"閘236之一輸入，其輸出爲在線路238之輸出信號，用以控制輸入級41之開關50。開關50也控制電路34之操作模式。"反及"閘236之另一輸入予以連接爲在線路134接收來自圖10中所示之模式解碼器電路110之輸出。在線路134之信號在已除時鐘脈衝之第三計數在線路100出現後變高。

D-型觸發器135之反相輸出予以連接爲設定一由"反及"閘240及241所構成之觸發器。觸發器在線路187藉來自脈衝發生器電路130之信號予以重設，對應於在輸出線路100之已除時鐘脈衝之計數八。來自觸發器之輸出予以連接至"反或"閘242之輸入，其連接爲在線路134接收在其另一輸入之信號。

在線路244之輸出啓動信號連接爲啓動以下所說明之輸出控制電路125。因此，在操作時，模式控制電路160防止在線路244之輸出啓動信號變高，及啓動輸出控制電路125之啓動輸出，直到在線路100已除時鐘脈衝之八計數之一段短停滯時間以後。

圖13中示以上配合模式解碼器電路110之說明所述之過渡計數器電路165，並有三D-型觸發器190-192。如果來自模式控制電路160之信號LDT-B保持低，第一D-型觸發器190藉鎖存受微斯特數據之狀態改變在線路250出現在樣本觸發器電路120之輸出予以計時。在LDT-B變高時，制止"或"閘195通過另外之過渡信號。第一D-型觸發器190之輸出予以連接至第二D-型觸發器191之時鐘輸入，以及連接

五、發明說明（25）

至三輸入"反或"閘196之第一輸入。第一D-型觸發器190之反相輸出予以連接至其數據輸入。

第二D-型觸發器192予以相似連接，其反相輸出連接至其輸入，並且其輸出連接至"反或"閘196之第二輸入及連接至第三D-型觸發器192之時鐘輸入。第三D-型觸發器192以相似方式與其連接至其輸入之反相輸出連接；然而；反相輸出也連接至三輸入"反或"閘196之第三輸入。

三D-型觸發器190-192藉在輸出線路133自模式解碼器電路110所產生之信號(圖10)予以重設，其在以上所說明之線路100在已除時鐘脈衝之第三計數變低。因此，過渡計數器165用以計數取樣受微斯特數據之四正緣，並在一長停滯時間週期後操作，以"叫醒"電路。簡言之，雖然以下詳細說明電路之叫醒特色，但如果在重設信號出現在線路133前達到計數四，輸出便在線路166變高，以下面所說明之方式叫醒電路之其餘部份。

在線路250至過渡計數器電路之輸入BNRZ也加至輸出控制電路125，圖14中示其細節。輸出控制電路125接收來自取樣或鎖存觸發器121之解碼BNRZ信號進入一啓動"及"閘252，其有輸出由輸出緩衝器253予以緩衝，以在數據出線路255提供數據出信號(DOUT)。"及"閘252由輸出啓動信號予以啓動，其爲在線路244由以上參照圖12所說明之模式控制電路160之"反或"閘242之輸出所產生。

在線路257之觸發器或定時輸出(TRIG)由啓動之"及"閘260所產生，其輸出由輸出緩衝器261予以緩衝。"及"閘

五、發明說明（ 26）

260也在線路244由來自模式控制電路160之"反或"閘242之輸出啓動信號予以啓動。至"及"閘260之另一輸入得自來自振盪器35在線路87所產生，延遲一半週期之時鐘信號。在線路87之時鐘信號由反相器265予以反相，以在線路117對以上參照圖 9 所說明之除2 計數器105所產生，進入D-型觸發器268之樣本命令信號計時。

在線路87之時鐘脈衝之半週期延遲係由D-型觸發器270所產生，其在其數據輸入接收來自D-型觸發器268之輸出及在線路87在其時鐘輸入接收時鐘脈衝。來自D-型觸發器270之輸出予以連接至"反或"閘271之一輸入，其輸出予以連接至"及"閘260。至"反或"閘271之另一輸入爲來自D-型觸發器268之輸出，其由反相器272予以反相。

在輸出線路257所產生之定時脈衝予以在除2 計數器105之輸出(並因此在線路250之二進制NRZ信號)，自在線路117之樣本命令信號之狀態改變延遲在線路87之時鐘信號之一半週期延遲可例如約爲10微秒。輸出定時脈衝於是爲時鐘信號在線路87之一半週期，也約爲10微秒。

除了在線路257之定時信號輸出予以延遲在線路100已除時鐘脈衝週期之一半週期外，在數據出線路255及定時信號輸出線路257之波形爲取樣觸發器120之BNRZ（二進制不歸零）輸出及在來自除2 電路105輸出之輸出之取樣脈衝之拷貝。

對照於以下所說明之正常電路操作，定時回復及曼徹斯特數據解碼系統34提供一測試模式，在此模式，一測試信號

五、發明說明（ 27）

可經由圖15中所示之測試模式控制電路55加至電路。因此，電路34正常在模式控制電路160之控制下，在其多模式輸入級41接收包含信號(MDAT)之曼徹斯特數據，圖12中示其細節。但爲提供測試操作模式，請再次參照圖15，來自多模式輸入級41之輸出在線路42連接至"反及"閘210，"反或"閘211，及多工器電路212之輸入。來自"反及"閘210及"反或"閘211之輸出分別藉反相器214及215予以反相，並可使用供希望之測試或監視目的。

如以上所討論，多工器電路212正常在線路42在其在至其餘電路之線路88之輸出產生包含信號之曼徹斯特數據。然而，如果高測試啓動信號加至測試啓動線路220，加在線路221包含測試信號之曼徹斯特數據便傳送至輸出線路88。

如以上所指示，依容納於輸入信號之曼徹斯特數據所建立之狀況而定，定時回復及曼徹斯特數據解碼系統34有三操作模式。依輸入信號之特性及性質而定，三操作模式提供操作之自適應界限檢測方案。第一操作模式爲如以上所說明之"穩態"模式，在此模式，包含曼徹斯特編碼數據流

五、發明說明（28）

路偏壓也保持。

電路操作之特定模式依開關50及58如何偏壓比較器46而定。因此，開關50及58操作，依據自監視曼徹斯特過渡指示波形所檢測到之信號狀況，響應在圖12中所示模式控制電路160在線路238之信號，而選擇三參考電壓之一。

在圖16a-c中略示產生供三參考電壓設定之波形。也請再次參照圖5，便明白在節點2 在比較器46之反相輸入之時間常數遠大於在節點1 在比較器46之非反相輸入。因之，節點2 主要響應DASK（解調ASK）信號之長期平均，而節點1 響應DASK數據過渡。在具有圖16a中所示波形之"穩態"操作模式，開關50接通並且開關58斷開。在"穩態"模式，參考電壓300在節點2 將會等於在節點1 之信號302之平均值。由於曼徹斯特數據之平均值始終中心在高與低電平之間，故達到最大雜訊免受性。

在具有圖16b中所示波形之"保持"模式，開關50及58均斷開。由於無放電路徑，電容器60在節點2 保持見爲波形304之先前電壓。供包含數據脈衝串，分開短停滯時間間隔，諸如波形306所示之傳輸格式，"保持"模式保持有效數據脈衝串間之最佳界限。

在具有圖13c中所示波形之"補償"模式，在節點2 之參考電壓308在節點1 自雜訊之平均值補償。補償電壓選擇爲致使參考選擇爲約在節點1 所預期有效信號310之高及低電平之中點。在長停滯時間間隔使用此模式。比較器輸出雜訊被壓制遠低於在參考電壓允許變爲等於雜訊平均值

五、發明說明（ 29）

之大多數遙控接收機所見者。

雖然在"補償"模式之比較器雜訊免受性可能不及在"穩態"模式良好，但簡單之傳輸格式與另外之信號處理合併，幾乎可消除偽叫醒順序在數據出線路255（圖14）後隨雜訊之可能性。可使用一種諸如圖17中所示具有叫醒順序及短停滯時間間隔之格式。吾人可看出，叫醒順序包括若干相似之脈衝過渡314-323，後隨一停滯時間間隔326，其復後隨希望之曼徹斯特數據流328，330。在例示之實施例，發出8 曼徹斯特過渡328之初始順序，以保證適當同步，但此非絕對必要。在使順序328同步後，便傳輸所討論之實際曼徹斯特數據330。利用此格式，在線路255之數據出及在輸出線路257來自輸出控制電路125之定時脈衝(圖14)便僅在有效叫醒順序及短停滯時間已出現後才作用。其將會保持作用直到檢測到另一停滯時間間隔。

模式控制電路160響應曼徹斯特過渡指示脈衝及在線路100之已除時鐘脈衝，以確定適當之比較器參考模式。在長停滯時間，執行"補償"模式，並且任何檢測到之過渡指示脈衝之過渡開始一候選叫醒順序。比較器46保持在"補償"模式，直到檢測到有效叫醒。有效叫醒由預定數之適當間開順序過渡所組成。爲供適當間開，任何二過渡間之分開必須少於三符號寬度。此係在所有過渡後計數在線路100之計數已除時鐘脈衝所確定。如果計數達到三，順序予以捨棄，並在次一檢測到之過渡開始。

更詳細而言，如圖8中所示，更詳示在輸入電路41之不

五、發明說明（ 30）

同節點之波形。在叫醒順序時，供比較器46之參考充電至曲線區段340所示信號平均加補償之最後值。在叫醒後，參考切換至在點342之"正常"模式。自該圖看出，在叫醒時，參考較之如果使用"穩態"模式更快速充電至平均值。此係由於減少之時間常數及補償電壓之存在。由於在例示之實施例在叫醒脈衝串有十二過渡，但僅四過渡需要叫醒，系統通常將會在整個脈衝串完成前被叫醒。雖然這允許供參考之另外時間，以回復至眞平均值，但如果其在"穩態"模式切入時已接通，則爲顯然有利。對於叫醒可能靠近或在叫醒脈衝串結尾出現之很微弱信號或高雜訊狀況，尤其如此。

在電路已叫醒後，在部位344出現短停滯時間。（請予察知，爲供例證目的，圖18中所例示之停滯時間部位344已予縮短。代表性停滯時間可例如約爲2 微秒，或較長。）在線路255之數據出信號及在線路257之定時脈衝在叫醒後之短停滯時間結尾予以啓動。此種隔開防止自叫醒脈衝串之其餘部份輸出數據。在每一曼徹斯特過渡脈衝後，在線路100計數已除脈衝，藉以檢測短停滯時間。如果計數達到三，便開始一短停滯時間，並且比較器參考切換至保持模式。此等設定保持有效，直到檢測到之過渡恢復或在輸出線路100之已除時鐘脈衝之計數達到64。如果檢測到之過渡首先出現，在輸出線路100之已除時鐘脈衝之計數予以設定至零，比較器參考予以設定至"穩態"模式，輸出予以啓動，並且解碼數據及定時脈衝或觸發出現在個別輸

五、發明說明（ 31）

出線路255及257。

雖然本發明業已以一定程度之特殊性予以說明及例示，但請予瞭解，本案揭示僅意在作爲實例，精於此項技藝者在諸部份之組合及配置可採取很多改變，而不偏離如下文所述之本發明之精神及範圍。

四、中文發明摘要（發明之名稱：將諸如曼徹斯特或類似編碼數據之雜訊及斷續數據解碼之方法及裝置）

根據本發明之一廣義方面，提供一種供解碼曼徹斯特編碼數據流之裝置(34)，該裝置包括一過渡檢測器(45)，供接收曼徹斯特編碼數據流，以在檢測到曼徹斯特編碼數據流之過渡時產生一過渡指示輸出。也提供一電路(105)，以在過渡指示輸出產生後之預定時間產生輸出控制脈衝。一取樣觸發器(120)接收曼徹斯特編碼數據流，並受輸出控制脈衝所控制，以在輸出控制脈衝產生時輸出一曼徹斯特編碼數據之狀態至輸出控制電路(125)。在一種較佳實施例，取樣觸發器(125)操作，以產生曼徹斯特編碼數據流之二進制NRZ形式。過渡檢測器(45)可構形爲使過渡指示輸出與一時鐘脈衝流之脈衝同步，並且也可包括一選相器，以選擇曼徹斯特數據之第一或第二符號至裝置之輸出。

英文發明摘要（發明之名稱：）

A5
B5

四、中文發明摘要（發明之名稱：METHOD AND APPARATUS FOR DECODING NOISY, INTERMITTENT DATA, SUCH AS MANCHESTER ENCODED DATA OR THE LIKE）

According to a broad aspect of the invention, an apparatus (34) for decoding a Manchester encoded data stream is provided. The apparatus includes a transition detector (45) for receiving the Manchester encoded data stream to produce a transition indicating output when a transition of the Manchester encoded data stream is detected. Also, a circuit (105) is provided to generate an output control pulse a predetermined time after the transition indicating output is produced. A sampling flip-flop (120) receives the Manchester encoded data stream, and is controlled by the output control pulse to output a state of the Manchester encoded data to an output control circuit (125) when the output control pulse is generated. In a preferred embodiment, the sampling flip-flop (125) operates to generate a binary NRZ form of the Manchester encoded data stream. The transition detector (45) may be configured to synchronize the transition indicating output with a pulse of a clock pulse stream, and also may include a phase selector to select either the first or second symbol of the Manchester data to the output of the apparatus.

（請先閱讀背面之注意事項再填寫本頁各欄）

裝

訂

六、申請專利範圍

1.一種供解碼曼徹斯特編碼數據流之裝置，包含：

一過渡檢測器，供接收曼徹斯特編碼數據流，以在檢測到曼徹斯特編碼數據流之過渡時產生過渡指示輸出；

一電路，在過渡指示輸出產生後之預定時間產生輸出控制脈衝；

一取樣觸發器，接收曼徹斯特編碼數據流，受輸出控制脈衝所控制，以在輸出控制脈衝產生時輸出曼徹斯特編碼數據之狀態。

2.根據申請專利範圍第1項之裝置，其中上述取樣觸發器操作，以產生二進制NRZ形式之曼徹斯特編碼數據流。

3.根據申請專利範圍第1項之裝置，另包含一時鐘發生器，供在頻率高於曼徹斯特編碼數據流產生一時鐘脈衝流。

4.根據申請專利範圍第3項之裝置，其中上述過渡檢測器連接爲接收時鐘脈衝流，並構形爲使過渡指示輸出與時鐘脈衝流之脈衝同步。

5.根據申請專利範圍第1項之裝置，另包含一選相器，以選擇在過渡後所出現之曼徹斯特數據單元之已知一半。

6.根據申請專利範圍第5項之裝置，其中上述選相器選擇曼徹斯特數據單元之第二一半。

7.根據申請專利範圍第5項之裝置，其中上述選相器選擇性曼徹斯特數據單元之第一一半。

8.根據申請專利範圍第7項之裝置，另包含一使來自觸發器之輸出反相之反相器。

六、申請專利範圍

9.一種定時回復及曼徹斯特數據解碼系統，包含：

一振盪器，提供輸出脈衝；

一多模式輸入電路，連接爲接收可包含曼徹斯特編碼數據信號之輸入信號，並輸出一包含信號之數據；

一過渡檢測器，連接爲接收來自多模式輸入電路之輸出信號，供在所有曼徹斯特數據過渡產生曼徹斯特過渡指示脈衝；

一曼徹斯特過渡計數器電路，連接爲接收來自振盪器之輸出脈衝，以在曼徹斯特數據過渡後產生預定數之振盪器脈衝；

一除2 電路，連接爲接收來自曼徹斯特過渡計數器電路之振盪器脈衝，以產生一樣本命令信號；

以及一取樣電路，連接爲接收來自除2 電路之輸出及曼徹斯特編碼數據，以響應來自除2 電路之輸出鎖存曼徹斯特編碼數據之狀態。

10. 根據申請專利範圍第9項之定時回復及曼徹斯特數據解碼系統，另包含：

一脈衝發生器電路，連接爲接收來自振盪器之輸出脈衝並產生其輸出計數；

一模式解碼器電路，連接爲接收來自脈衝發生器電路之輸出計數，以在來自脈衝發生器電路之輸出計數之預選計數提供輸出；

以及一模式控制電路，連接爲接收模式解碼器電路之至少有些輸出，模式控制電路連接爲選擇性控制多模式

六、申請專利範圍

輸入電路之模式。

11. 根據申請專利範圍第10項之定時回復及曼徹斯特數據解碼系統，其中上述模式解碼器電路爲一邏輯閘陣列。

12. 根據申請專利範圍第9項之定時回復及曼徹斯特數據解碼系統，另包含：

一輸出控制電路，連接爲接收取樣電路所鎖存之數據及過渡指示脈衝，供產生一NRZ輸出數據信號及輸出定時脈衝。

13. 根據申請專利範圍第12項之定時回復及曼徹斯特數據解碼系統，另包含一延遲輸出定時脈衝一半週期之電路。

14. 根據申請專利範圍第9項之定時回復及曼徹斯特數據解碼系統，其中上述多模式輸入電路有一"穩態"模式，在此模式，一包含曼徹斯特編碼數據流之信號予以處理，並且在輸出產生輸出二進制NRZ信號，一"補償"模式，在此模式，需要出現叫醒曼徹斯特數據順序導使電路"叫醒"，以採取並恢復"穩態"操作模式，及一"保持"模式，在此模式，即使未收到"穩態"模式曼徹斯特編碼數據，電路偏壓也保持。

15. 根據申請專利範圍第9項之定時回復及曼徹斯特數據解碼系統，另包含一測試模式控制電路，供控制輸入信號抑或測試信號予以處理。

16. 根據申請專利範圍第9項之定時回復及曼徹斯特數據解碼系統，其中上述多模式輸入電路包含：

六、申請專利範圍

一比較器，有反相及非反相輸入；

一第一電阻器，輸入信號藉其連接至非反相輸入；

一第二電阻器，輸入信號藉其連接至反相輸入；

一第一開關功能，與第二電阻器串聯；

一第三電阻器，在一端連接至比較器之反相輸入；

一第二開關功能，連接在第三電阻器之另一端與一參考電壓之間；

一第一電容器，連接於比較器之反相與非反相輸入之間；

以及一第二電容器，連接於比較器之非反相輸入與接地之間；

第一及第二開關功能係受模式控制電路所控制。

17. 一種叫醒電路，供響應在輸入信號之曼徹斯特數據叫醒順序，自一靜止狀態開始操作一曼徹斯特編碼數據檢測器；包含：

一輸入電路，有一保持模式，其最初爲關閉，以在曼徹斯特編碼數據檢測器爲在靜止狀態時接收輸入信號，以產生一對應於輸入信號之取樣狀態之數據輸出信號；

一補償電路，其最初爲開啓，以接收輸入信號，以將輸入信號與一得自輸入信號平均值之參考電壓加一預定補償電壓比較，以產生一對應於參考電壓與輸入信號間之差異之數據輸出信號；

一電路，供確定在來自樣本及保持電路之數據輸出信號是否已收到可能之曼徹斯特編碼數據單元，以選擇性

六、申請專利範圍

接通補償電路；

以及一電路，供確定是否已順序收到預定數之數據單元具有補償電路之數據輸出信號內之個別預定狀態，以選擇性關斷補償電路。

18. 根據申請專利範圍第17項之叫醒電路，另包含一微分放大器，具有反相及非反相輸入及輸出，並且其中：

輸入電路包含一第一電容器，連接於反相輸入與參考電位之間，及一第二電容器連接於非反相輸入與參考電位之間，以及一第一電阻器連接於輸入信號與反相輸入之間，其中在微分放大器之輸出產生數據輸出信號；

補償電路包含一第一電阻器，連接於微分放大器之反相輸入與參考電壓之間，第二電阻器連接於反相輸入與輸入信號之間，以及一開關與第二電阻器串聯連接，以開啓補償電路，其中微分放大器之輸出在第一開關接通時產生對應於參考電壓與輸入信號間之差異之數據輸出信號；以及

微分電路包含一第二開關與第二電阻器串聯，其中在第二開關接通並且第一開關斷開時，輸出微分放大器產生放大輸入信號。

19. 一種方法，供解碼曼徹斯特編碼數據，以產生數據之不歸零二進制表示法，包含：

產生一脈衝供曼徹斯特編碼數據之每一過渡；

產生一與脈衝在定時相位之取樣信號，供曼徹斯特編碼數據之每一過渡；

六、申請專利範圍

在每次出現取樣信號鎖存曼徹斯特編碼數據，並產生鎖存數據之輸出；

以及使用自適應界限檢測，以接收具有增強雜訊免受性之曼徹斯特編碼數據。

20. 根據申請專利範圍第19項之方法，其中上述使用自適應界限檢測之步驟包含在解碼電路之數據輸入級提供許多操作模式。

21. 根據申請專利範圍第20項之方法，其中上述提供許多操作模式之步驟包含提供"穩態"及"補償"操作模式。

22. 一種方法，供在曼徹斯特數據流產生對應於每一曼徹斯特單元之已知一半之狀態之NRZ數據信號，包含：

在曼徹斯特數據流在每一過渡產生一過渡脈衝；

產生一系列定時脈衝，在曼徹斯特數據流有一頻率爲曼徹斯特單元之n 倍頻率；

響應每一過渡脈衝重新開始系列定時脈衝；

在出現每一第m 定時脈衝時，鎖存曼徹斯特單元之目前狀態，其中m 大於n/2；

計數定時脈衝，以提供一定時脈衝計數；

響應每一過渡脈衝重新開始計數；以及

如果定時脈衝計數變爲大於n/2，進行鎖存，以在下次第(n/2)出現定時脈衝時鎖存曼徹斯特數據流。

23. 根據申請專利範圍第22項之方法，其中上述定時脈衝之頻率倍數爲曼徹斯特數據流之二倍頻率，並且其中n爲2。

六、申請專利範圍

24. 一種方法，供在曼徹斯特數據流產生一對應於曼徹斯特單元之第二半狀態之NRZ數據信號，包含：

產生系列定時脈衝，在曼徹斯特數據流有一頻率爲曼徹斯特單元之一半頻率；

在出現每一第二定時脈衝時鎖存一曼徹斯特單元之目前狀態；

檢測在曼徹斯特數據流出現二倍寬脈衝；

以及使鎖存重新同步，以在已檢測到二倍寬脈衝後在其次出之現定時脈衝開始。

25. 一種供在曼徹斯特數據流產生一對應於曼徹斯特單元之第二半狀態之NRZ數據信號之裝置，包含：

一振盪器，產生一時鐘脈衝流；

一脈衝發生器，連接爲接收曼徹斯特數據流，供在曼徹斯特數據流在每一過渡產生輸出脈衝；

一除n 計數器，連接爲由來自振盪器之時鐘脈衝予以計時，除n 計數器有一輸出在預定數之時鐘脈衝後改變狀態；

一定時觸發器，連接爲由來自除n 計數器之輸出予以計時，觸發器連接爲在來自除n 計數器之輸出之所有第二計數產生輸出；

一取樣觸發器，連接爲在定時觸發器之數據輸入及輸出在時鐘輸入接收曼徹斯特數據流，取樣觸發器在取樣觸發器予以計時時在輸出提供曼徹斯特數據流之狀態；

以及一順序計數器，連接爲在來自脈衝發生器時鐘之

A8
B8
C8
D8

六、申請專利範圍

輸入及輸出脈衝，在重設輸入接收除n 計數器之輸出，從而順序計數器產生一信號指示在何時已出現二倍寬曼徹斯特脈衝，信號係予連接爲重設取樣觸發器。

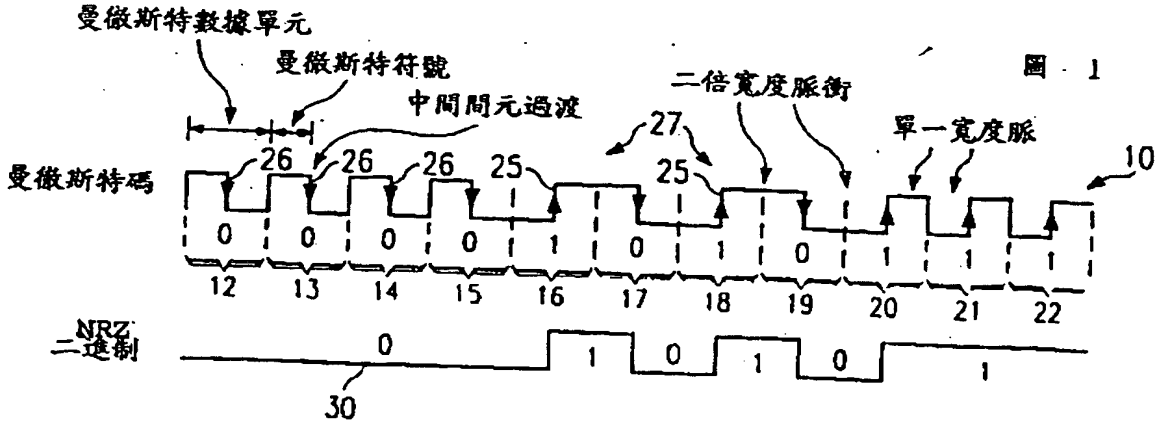

曼徹斯特數據單元
曼徹斯特符號
中間間元過渡
二倍寬度脈衝
單一寬度脈
曼徹斯特碼
NRZ
二進制
26
25
27
10
30

圖 1

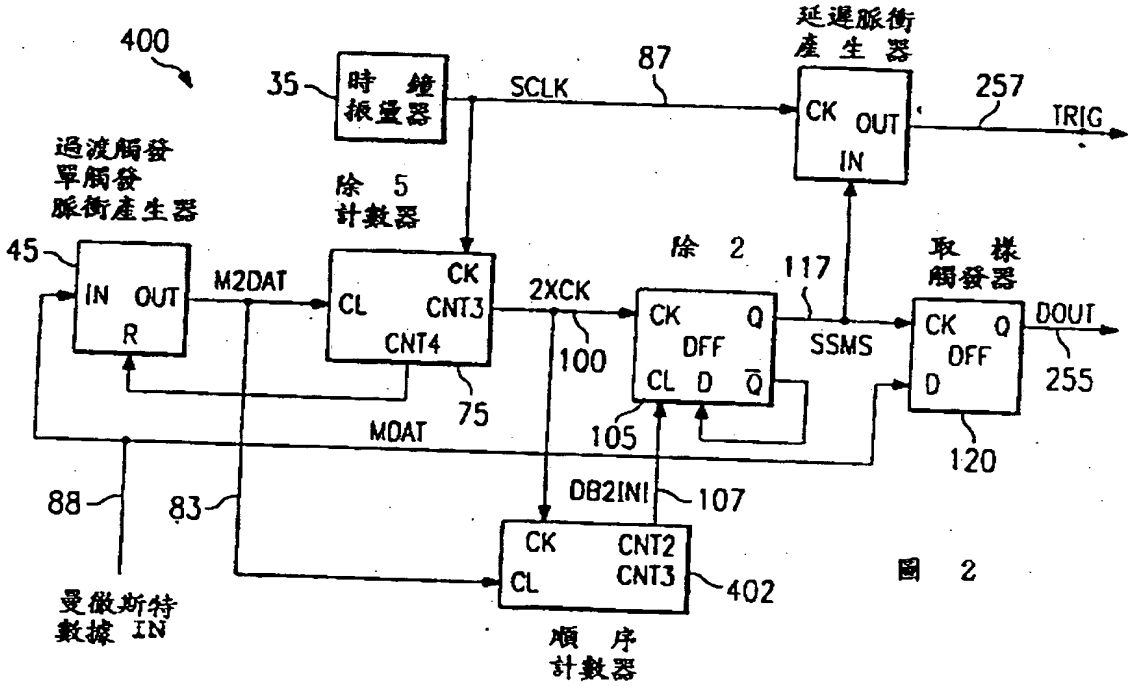

400
35
時 鐘
振盪器
SCLK
87
延遲脈衝
產 生 器
CK OUT
IN
257
TRIG
過渡觸發
單觸發
脈衝產生器
除 5
計數器
除 2
45
IN OUT
R
M2DAT
CK
CL CNT3
CNT4
2XCK
CK Q
DFF
CL D Q̄
117
SSMS
取 樣
觸發器
CK Q
DFF
D
DOUT
255
75
100
105
120
MDAT
88
83
DB2INI
107
CK CNT2
CL CNT3
402
曼徹斯特
數據 IN
順 序
計數器

圖 2

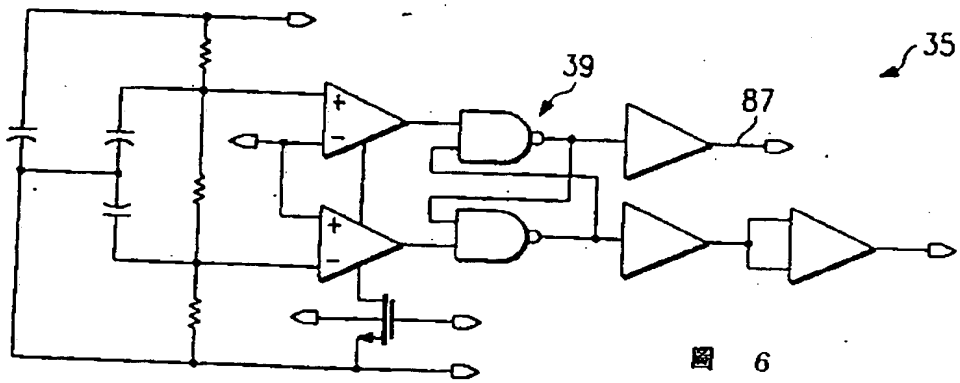

35
39
87

圖 6

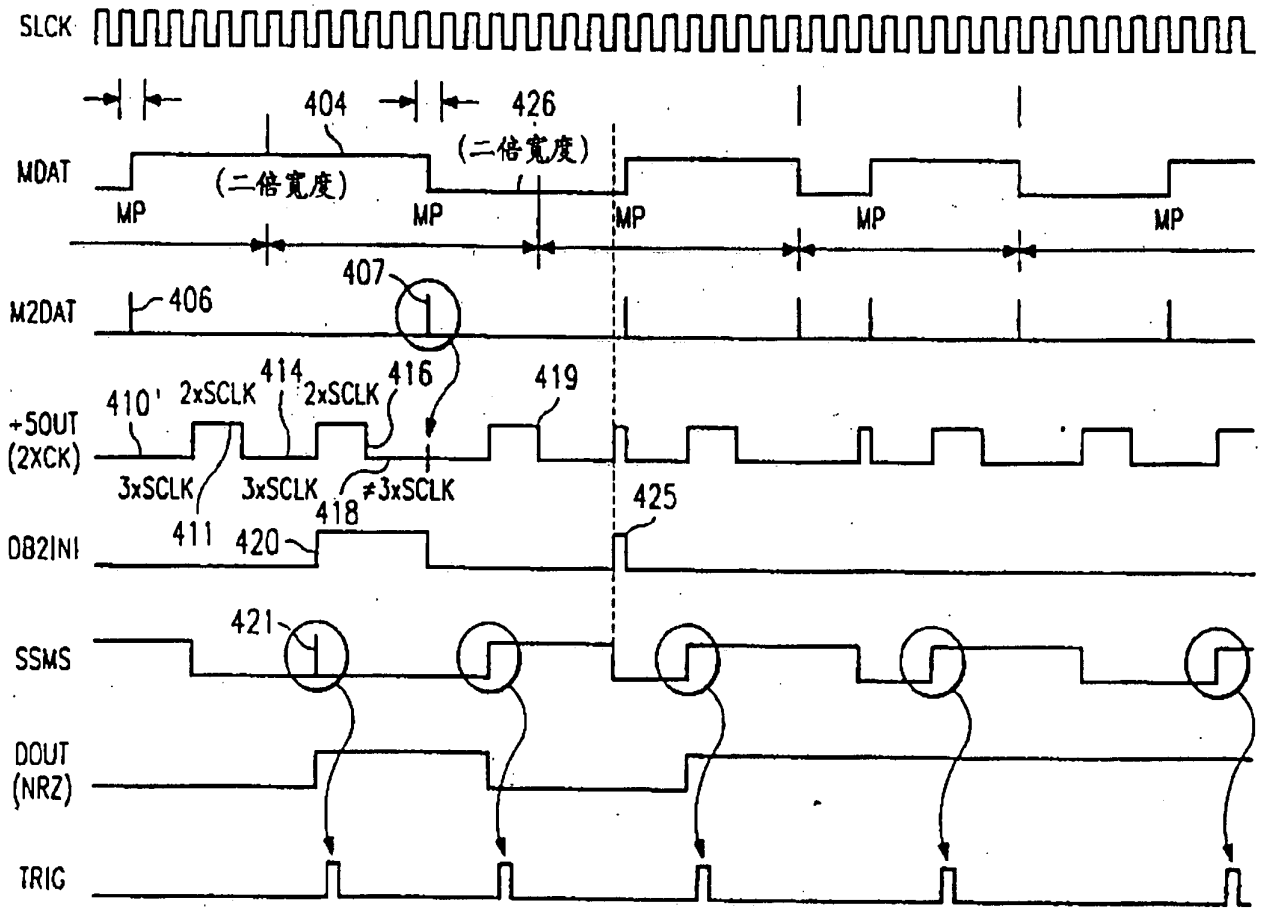

SLCK
404
426
(二倍寬度)
MDAT
(二倍寬度)
MP
MP
MP
MP
MP
407
M2DAT
406
414
416
419
410'
2xSCLK
2xSCLK
+5OUT
(2XCK)
3xSCLK
3xSCLK
≠3xSCLK
418
425
411
420
DB2INI
421
SSMS
DOUT
(NRZ)
TRIG

圖 3

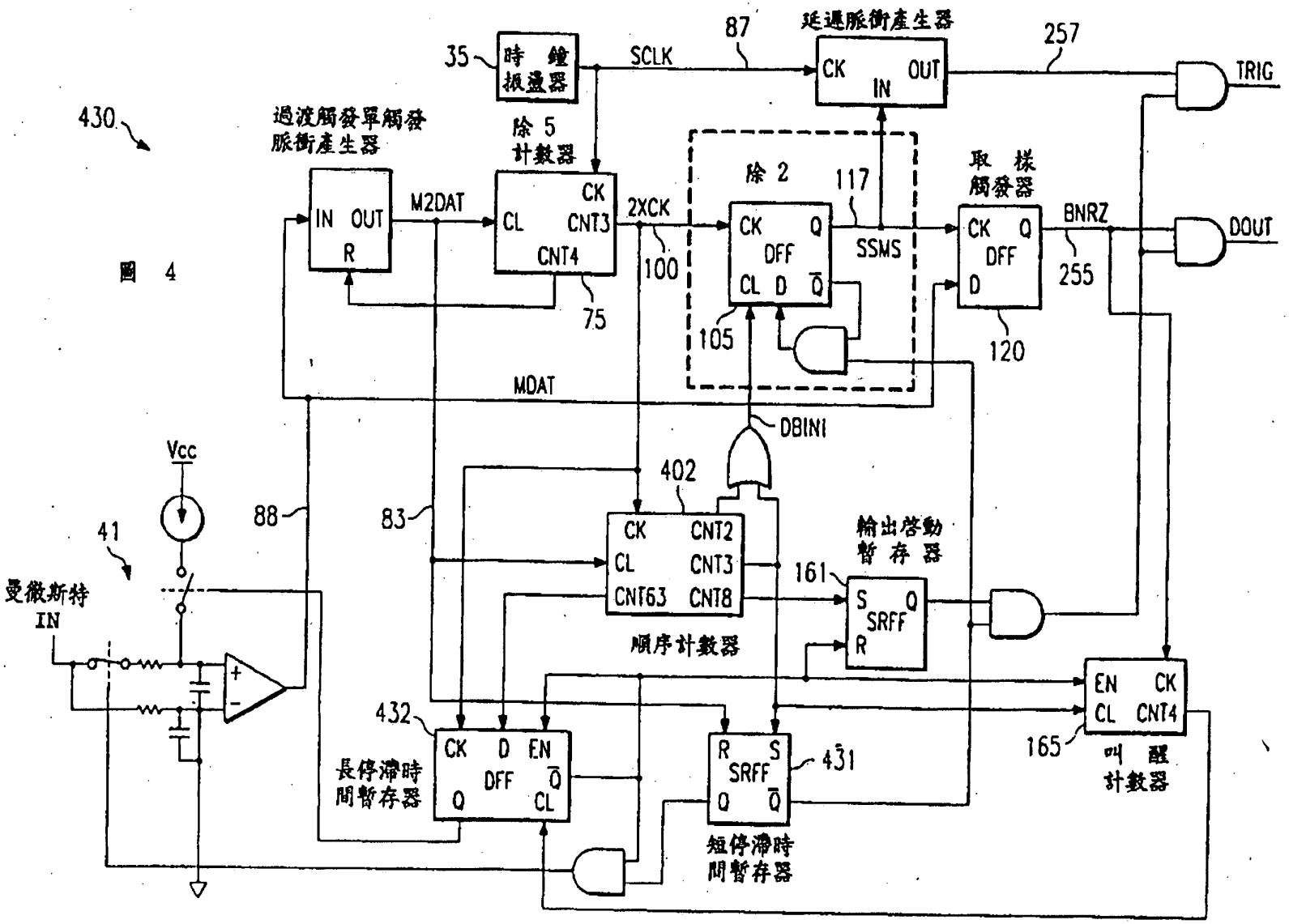
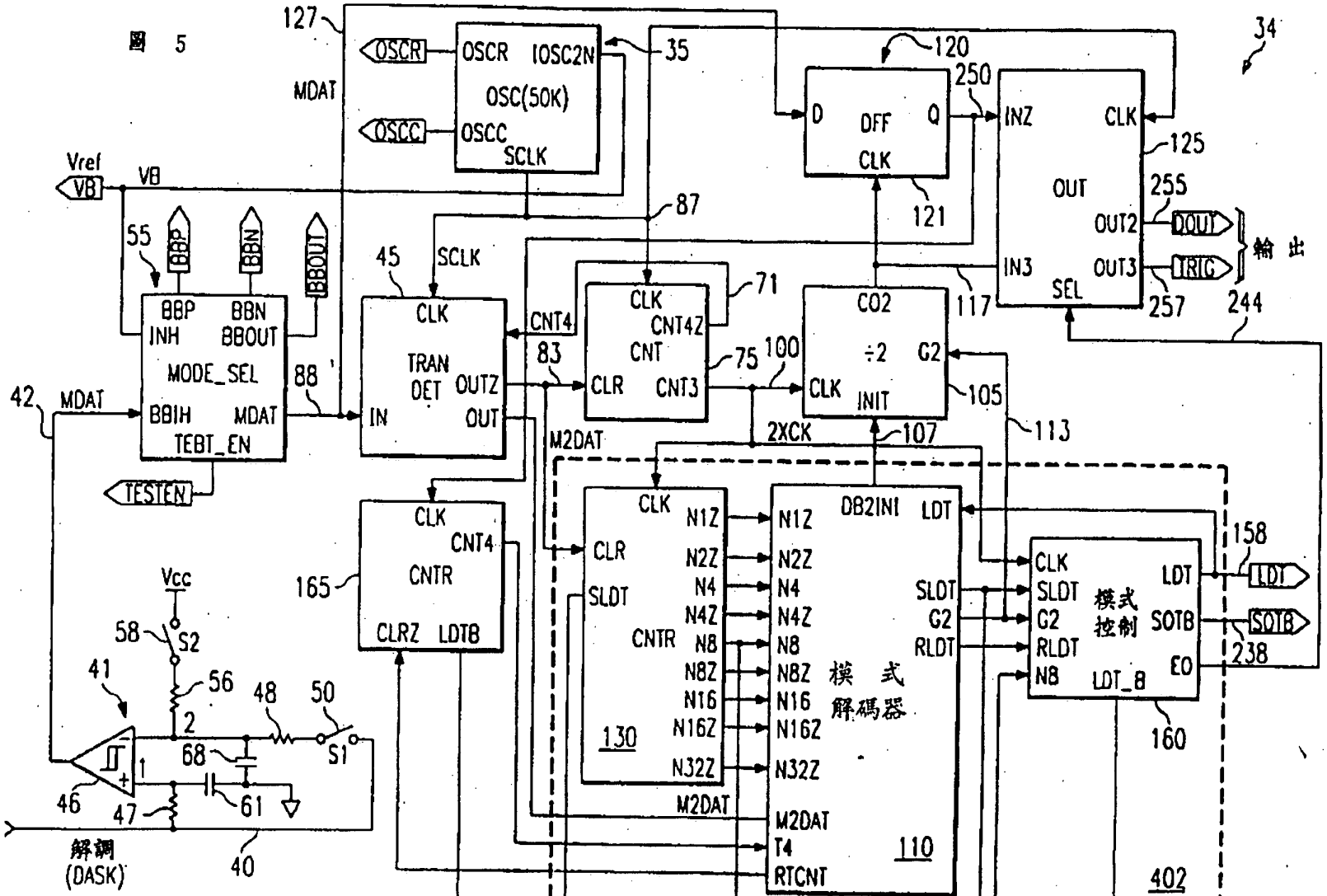

430
過渡觸發單觸發
脈衝產生器
35
時 鐘
振盪器
SCLK
87
延遲脈衝產生器
CK
IN
OUT
257
TRIG
除 5
計數器
IN
OUT
R
M2DAT
CK
CL
CNT3
CNT4
75
2XCK
100
除 2
CK
Q
DFF
CL
D
Q̄
105
117
SSMS
取 樣
觸發器
CK
Q
DFF
D
120
BNRZ
255
DOUT
MDAT
DBINI
402
Vcc
41
88
83
受微斯特
IN
CK
CNT2
CL
CNT3
CNT63
CNT8
順序計數器
輸出啓動
暫 存 器
161
S
Q
SRFF
R
EN
CK
CL
CNT4
165
叫 醒
計數器
432
CK
D
EN
DFF
Q̄
Q
CL
長停滯時
間暫存器
R
S
SRFF
431
Q
Q̄
短停滯時
間暫存器

圖 4

圖 5


127
OSCR
OSCC
OSCR IOSC2N
OSC(50K)
OSCC
SCLK
MDAT
35
120
250
D
DFF
Q
CLK
121
34
INZ
CLK
125
OUT
255
OUT2
DOUT
OUT3
TRIG
IN3
SEL
257
244
117
輸出
Vref
VB
87
55
BBP
BBN
BBOUT
45
SCLK
BBP
BBN
INH
BBOUT
MODE_SEL
BBIH
MDAT
TEBT_EN
88
42
MDAT
TESTEN
CLK
TRAN
DET
OUTZ
IN
OUT
CNT4
83
CLK
CNT4Z
CNT
CLR
CNT3
71
75
100
CO2
÷2
G2
CLK
INIT
105
107
113
2XCK
M2DAT
CLK
CNT4
CNTR
CLRZ
LDTB
165
CLK
N1Z
CLR
N2Z
SLDT
N4
N4Z
CNTR
N8
N8Z
N16
N16Z
N32Z
130
M2DAT
N1Z
N2Z
N4
N4Z
N8
N8Z
N16
N16Z
N32Z
M2DAT
T4
RTCNT
DB2INI
LDT
SLDT
G2
RLDT
模式
解碼器
110
CLK
SLDT
G2
RLDT
N8
模式
控制
LDT
SOTB
EO
LDT_B
158
LDT
SOTB
238
160
402
Vcc
58
S2
41
56
48
50
2
68
S1
1
46
47
61
解調
(DASK)
40

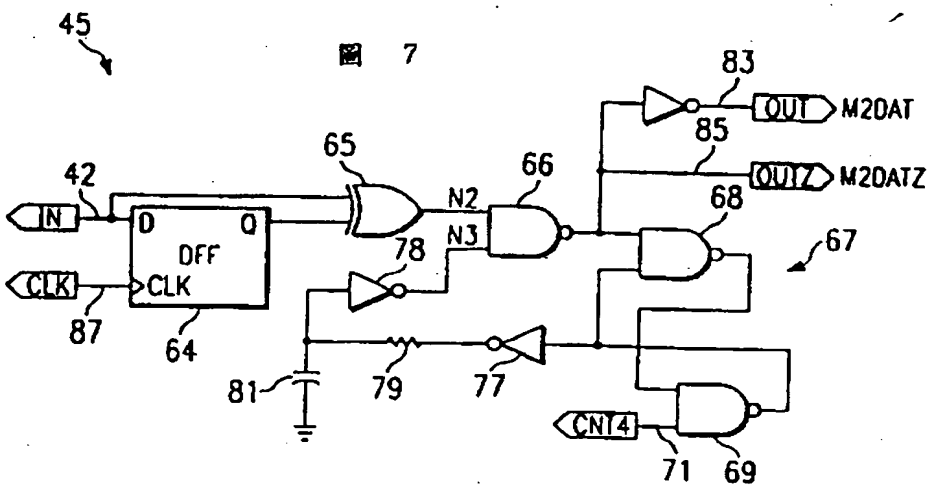

45
42
IN
CLK
87
D
Q
DFF
CLK
64
65
66
N2
N3
78
81
79
77
83
OUT
M2DAT
85
OUTZ
M2DATZ
68
67
CNT4
71
69

図 7

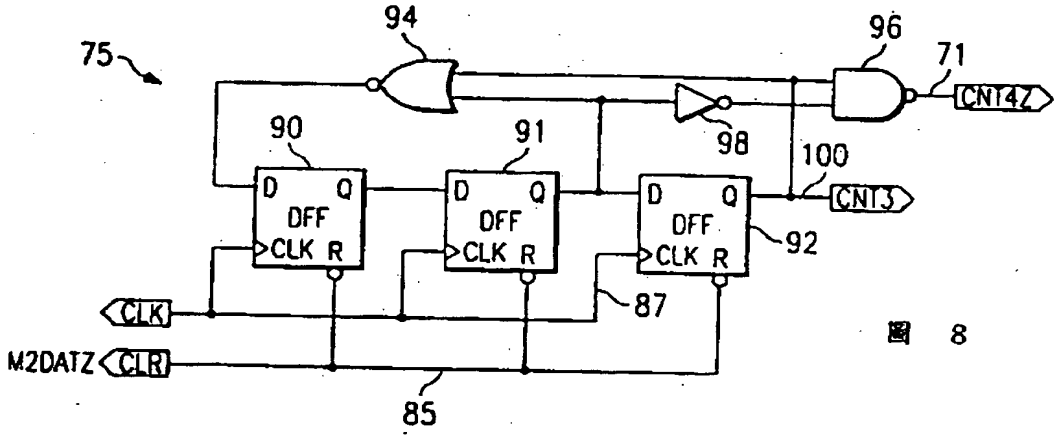

75
94
96
71
CNT4Z
98
90
91
100
CNT3
D
Q
DFF
CLK
R
92
87
CLK
M2DATZ
CLR
85

図 8

図 9

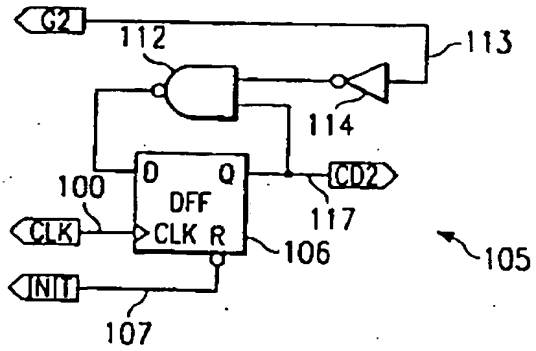

G2
112
113
114
100
D
Q
DFF
CLK
R
CD2
117
106
105
CLK
INIT
107

圖 10

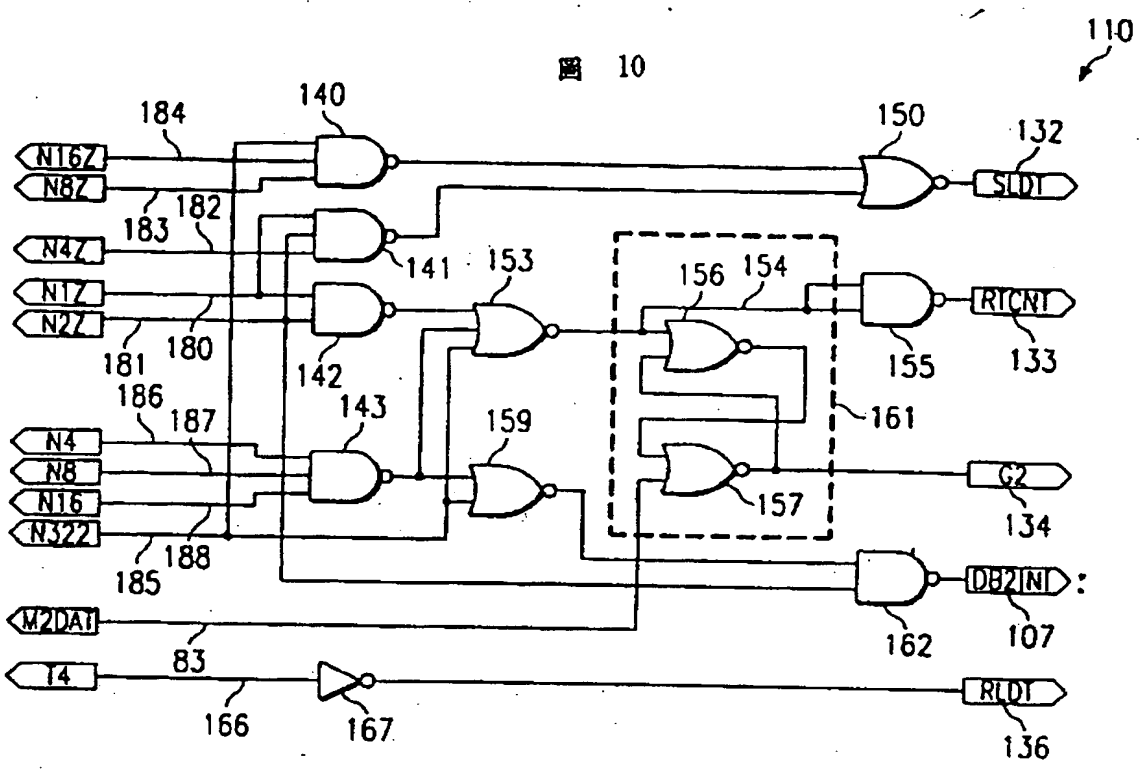
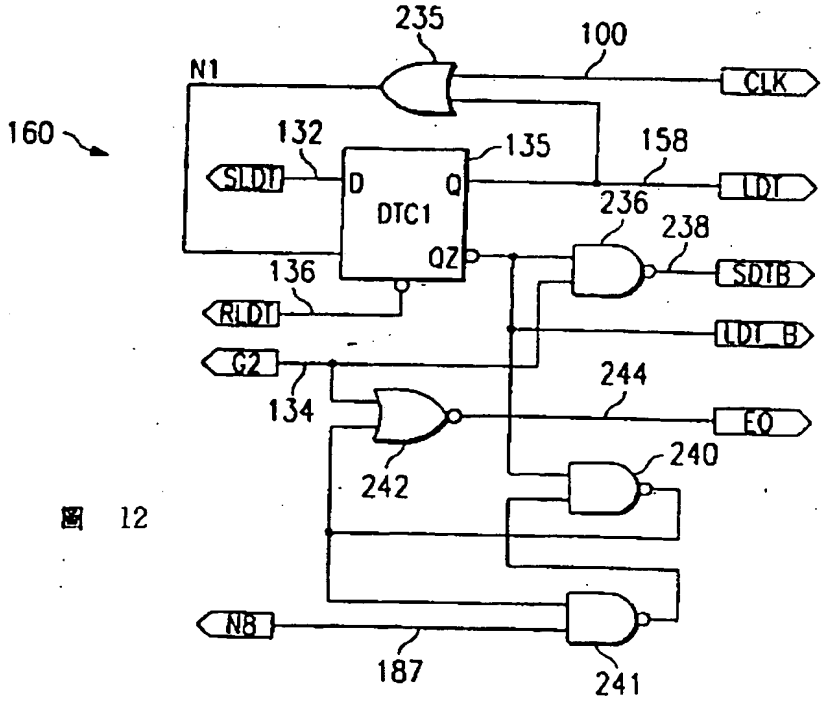

110
140
184
150
132
N16Z
N8Z
SLDI
182
183
N4Z
141
153
156
154
N1Z
N2Z
RTCNT
181
180
142
155
133
186
187
143
159
161
N4
N8
N16
N322
157
G2
134
188
185
DB2IN
107
M2DAT
162
83
T4
RLDT
166
167
136

圖 12


160
235
100
N1
CLK
132
135
158
SLDI
D
Q
DTC1
LDI
236
238
QZ
SDTB
136
RLDT
LDI_B
G2
244
134
EQ
240
242
N8
187
241

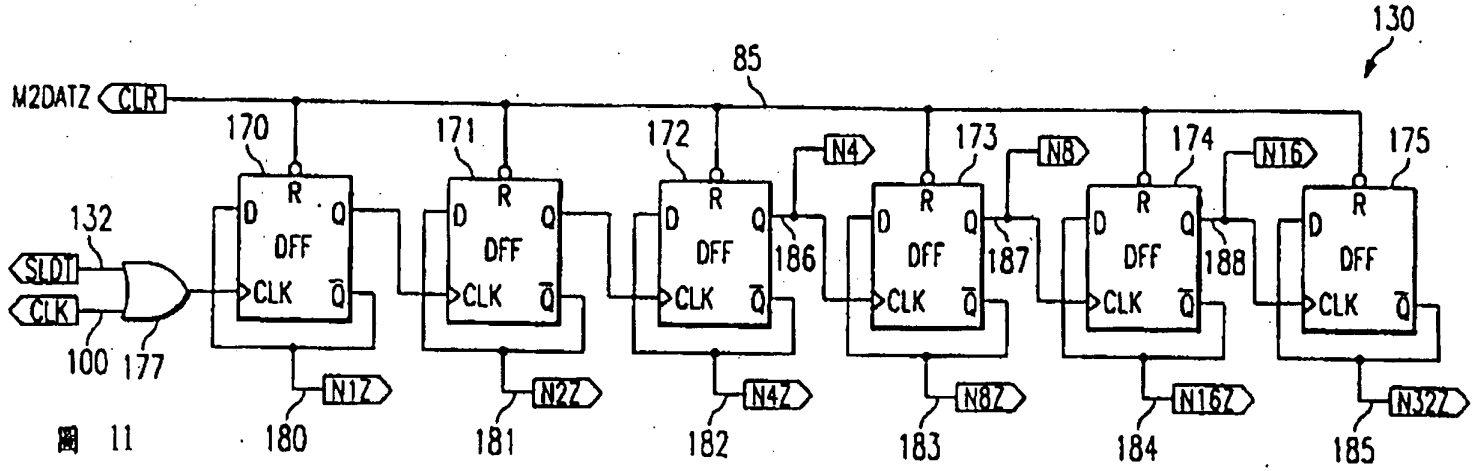

130
85
M2DATZ
CLR
170
171
172
173
174
175
N4
N8
N16
132
SLOT
CLK
100
177
D
R
Q
DFF
CLK
Q
186
187
188
N1Z
N2Z
N4Z
N8Z
N16Z
N32Z
180
181
182
183
184
185

圖 11

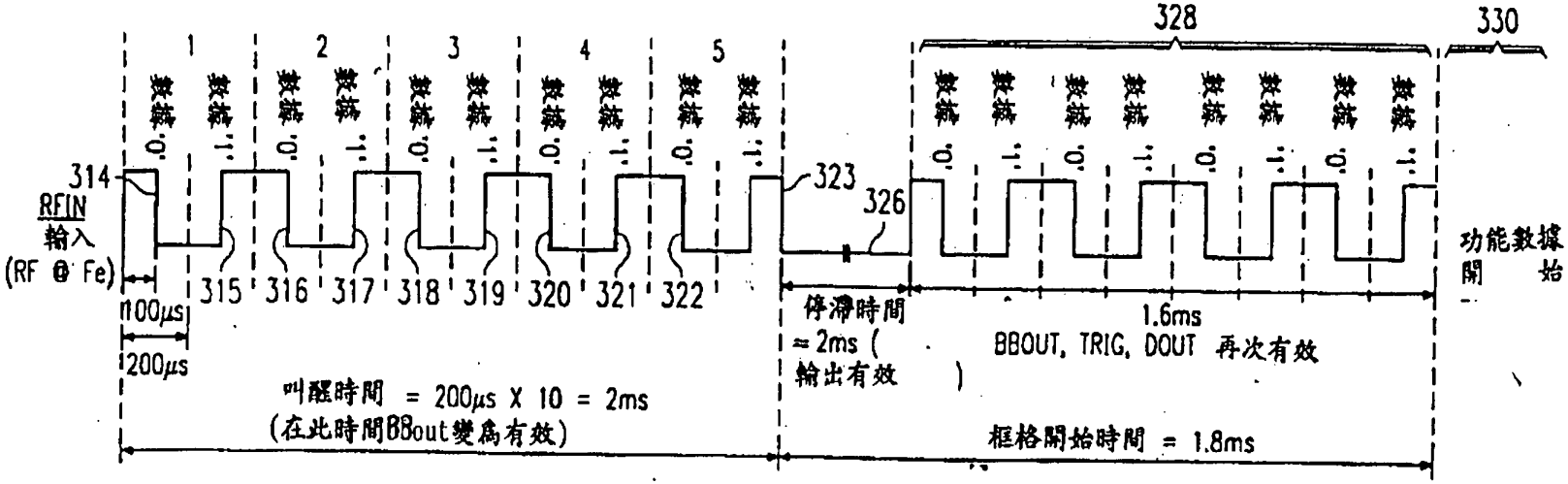

328
330
1
2
3
4
5
數碼 "0"
數碼 "1"
314
RFIN
輸入
(RF @ Fe)
315
316
317
318
319
320
321
322
323
326
100μs
200μs
叫醒時間 = 200μs X 10 = 2ms
(在此時間BBout變爲有效)
停滯時間
≈2ms (
輸出有效)
1.6ms
BBOUT, TRIG, DOUT 再次有效
框格開始時間 = 1.8ms
功能數據
開 始

圖 17

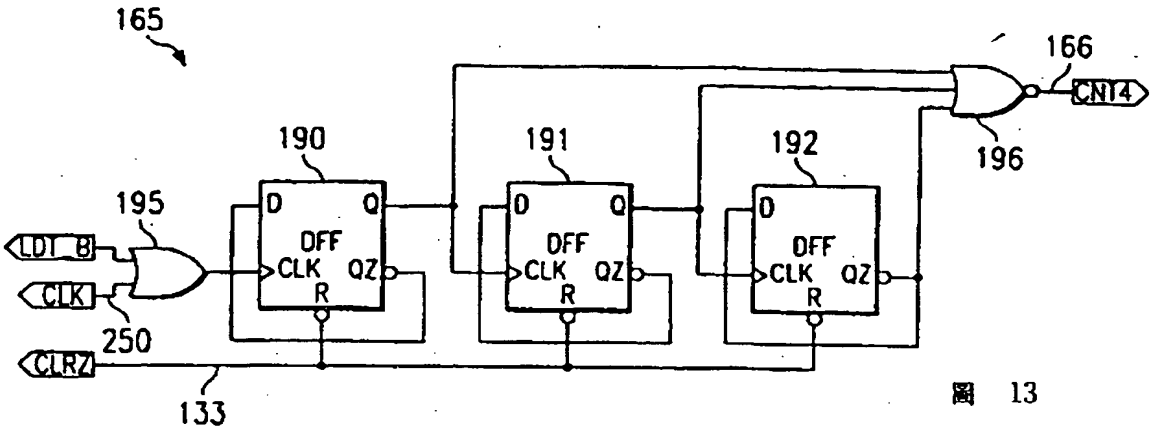

165
166
CNT4
196
190
191
192
195
D
Q
DFF
CLK
QZ
R
LDT_B
CLK
250
CLRZ
133

圖 13

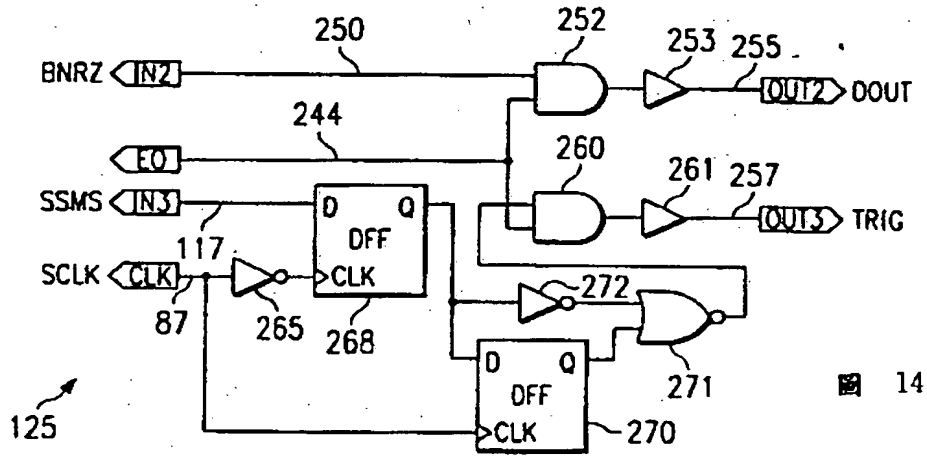

250
252
253
255
BNRZ
IN2
OUT2
DOUT
244
EO
260
261
257
SSMS
IN3
OUT3
TRIG
117
SCLK
CLK
87
265
268
272
271
270
125

圖 14

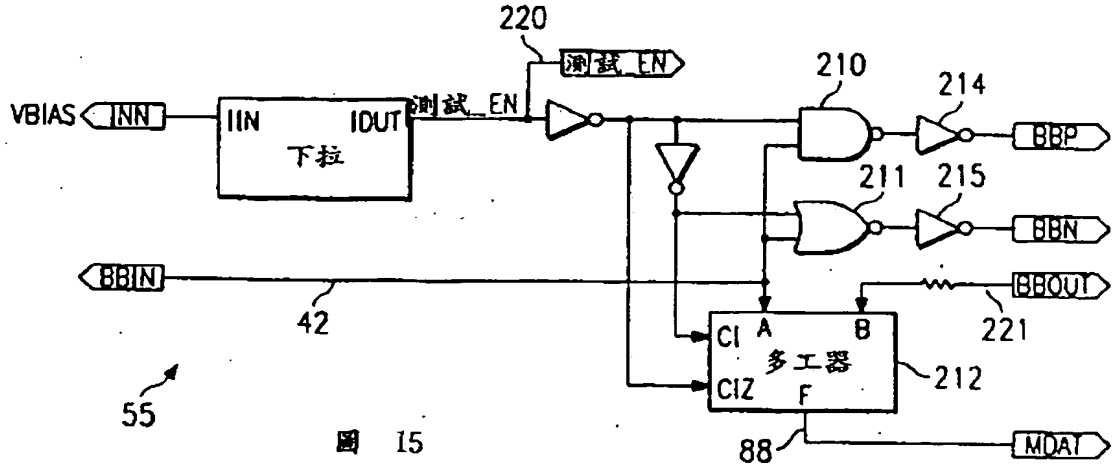

220
測試_EN
210
214
VBIAS
INN
IIN
IDUT
下拉
211
215
BBP
BBN
BBIN
BBOUT
42
221
CI
A
B
多工器
CIZ
F
212
55
88
MOAT

圖 15

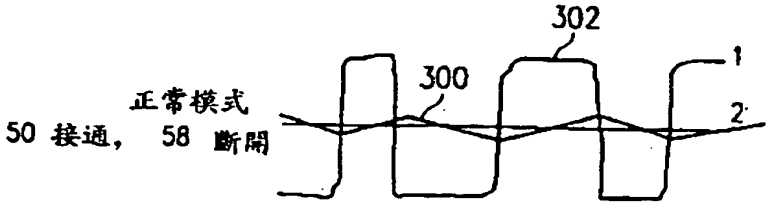


圖 16A

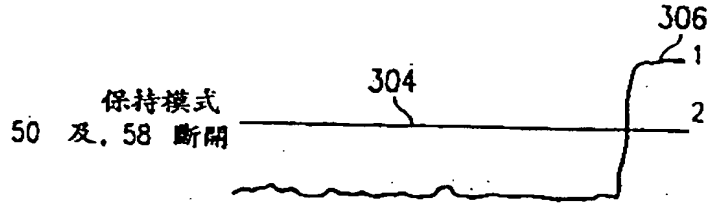


圖 16B

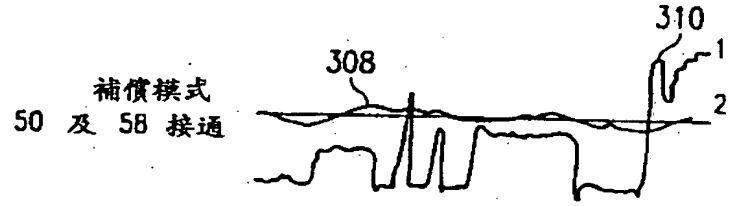


圖 16C

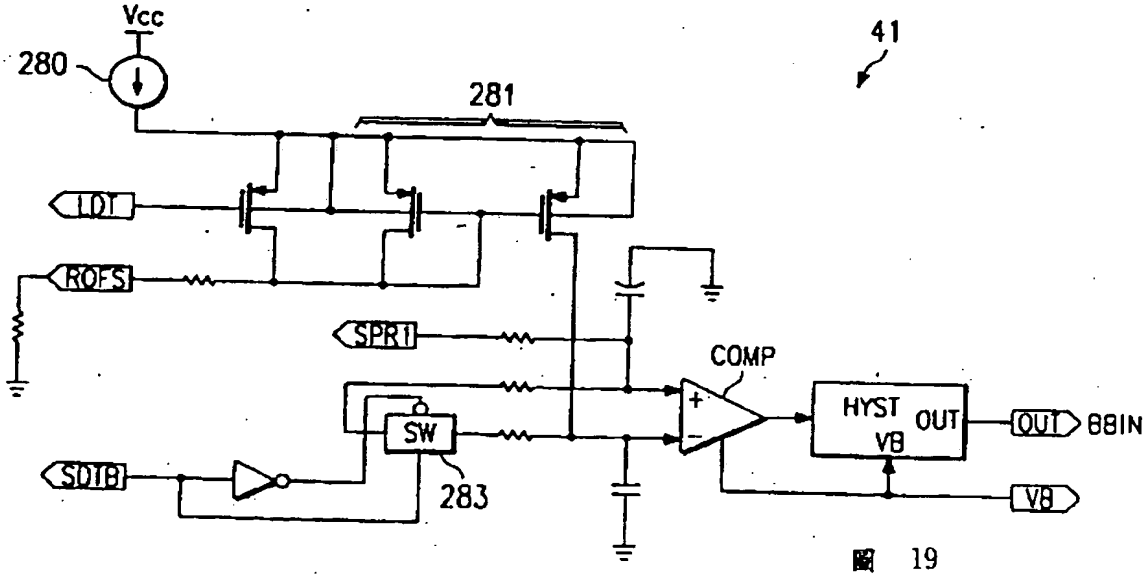


圖 19

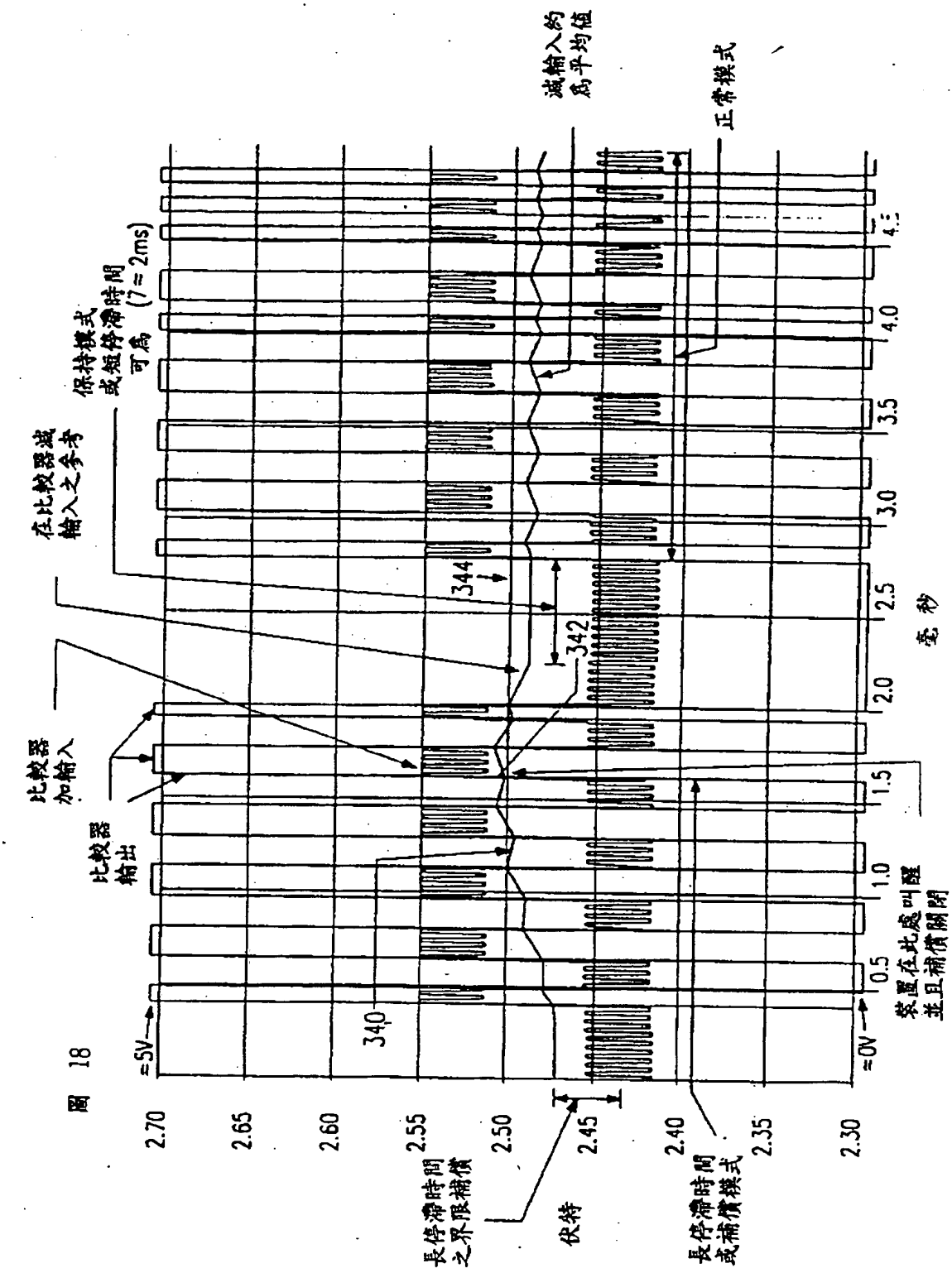

減輸入約為平均值
正常模式
保持模式或短停滯時間可為 (T= 2ms)
在比較器減輸入之參考
比較器加輸入
比較器輸出
=5V
=0V
340
342
344
2.70
2.65
2.60
2.55
2.50
2.45
2.40
2.35
2.30
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
毫秒
長停滯時間之界限補償
伏特
長停滯時間或補償模式
裝置在此處叫醒並且補償關閉

圖 18

Patent Application
TI-20092P

METHOD AND APPARATUS FOR DECODING NOISY, INTERMITTENT DATA, SUCH AS MANCHESTER ENCODED DATA OR THE LIKE

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

This invention relates to improvements in methods and apparatuses for decoding noisy, intermittent data, such as Manchester encoded data, or the like, and additionally relates to methods and circuits having multiple modes of operation depending upon the data signal that is received.

2. RELEVANT BACKGROUND

Manchester encoded data is useful for reliably transmitting telemetry and other types of data. Typically, for example, a Manchester encoded data stream may be generated from an encoded telemetry data stream, which may be, for example, a binary nonreturn-to-zero (BNRZ) encoded signal (or data stream encoded by another similar technique), known in the art. Upon receiving the Manchester encoded signal, the signal is decoded to recover the original BNRZ encoded signal. One of the problems inherent in data transmission by any means, especially via radio frequency transmissions, is that the signal becomes noisy, accumulating static, or other rf signals or noise. This makes decoding the Manchester signal difficult to reliably perform.

Manchester encoding, which is widely used in data transmission and telemetry fields, defines data states of the signal to be encoded by the direction of midpoint transitions in an encoding signal, which will become the Manchester encoded data stream. The Manchester encoded data stream has time sequential "cells" of equal duration. At the midpoint of each cell, the data changes state in a direction that indicates the state of the signal to be encoded.

Thus, for example, a transition from a high to low logic state indicates that the signal to be encoded is in a logic low

state. On the other hand, a transition from a low to high logic state indicates that the signal to be encoded is in a logic high state. Of course, at the end points of each cell, the state of the signal that will form the Manchester encoded data stream must be set up or established to enable the next midpoint transition. Thus, if a logic zero is to be encoded, the signal that will form the Manchester encoded data stream must be in an initial logic high state so that the midpoint transition from high to low can be realized. Alternatively, if a logic one is to be encoded, the signal that will form the Manchester encoded data stream must be in an initial logic low state so that the midpoint transition from low to high can be realized.

It can therefore be seen that if a series of logic states that are the same are encoded, the resulting Manchester encoded signal will be a square wave of period equal to the length of the cell. On the other hand, if a series of alternate logic ones and zeros are to be encoded, the resulting Manchester encoded signal will be a square wave of period equal to twice the length of the cell.

Various methods for decoding Manchester encoded data have been proposed. One popular technique is to use a phase locked loop circuit. In practice, however, sometimes a Manchester encoded signal is formatted to provide a "wake up" sequence, such as ten data cells, followed by a short dead time, followed by the actual data. Since the wake up sequence is so short, only 10 data cells, the circuit might not lock and might drift during the short dead time. Thus, the commonly used phase locked loop decoding technique cannot be used.

Other decoding techniques employ analog and digital matched filters, integrate and dump schemes, and highly over sampled digital signal processing techniques. Long synchronization time

and high component count preclude the use of most of these schemes.

One method that has been proposed employs a gating circuit that responds to the mid-cell transitions in a Manchester encoded waveform to produce an enabling signal. The enabling signal causes a clock circuit to generate high frequency clock pulses, which are accumulated in a programmable counter. If the counter exceeds a clock count threshold before the beginning of the following enabling signal, a storage element is caused to sample and store the encoded waveform.

SUMMARY OF THE INVENTION

In light of the above, therefore, it is an object of the invention to provide an improved circuit and method for Manchester data decoding and timing recovery.

It is another object of the invention to provide an improved circuit and method of the type described that has various modes of operation, depending upon the nature of the input signal.

It is another object of the invention to provide an improved circuit and method of the type described that has a "wake up" mode of operation in which no output is produced until a predetermined sequence of Manchester data is received.

It is another object of the invention to provide an improved circuit and method of the type described that has a "hold" mode in which a predetermined dead time period may occur in which no Manchester data is received, and during which the biases of the circuit are maintained.

These and other objects, features and advantages of the invention will be apparent to those skilled in the art from the following detailed description of the invention, when read in conjunction with the accompanying drawings and appended claims.

According to a broad aspect of the invention, an apparatus for decoding a Manchester encoded data stream is provided. The apparatus includes a transition detector for receiving the Manchester encoded data stream to produce a transition indicating output when a transition of the Manchester encoded data stream is detected. Also, a circuit is provided to generate an output control pulse a predetermined time after the transition indicating output is produced. A sampling flip-flop receives the Manchester encoded data stream, and is controlled by the output control pulse to output a state of the Manchester encoded data when the output control pulse is generated.

In a preferred embodiment, the sampling flip-flop operates to generate a binary NRZ form of the Manchester encoded data stream. The transition detector may be configured to synchronize the transition indicating output with a pulse of a clock pulse stream, and also may include a phase selector to select either the first or second symbol of Manchester data for latching and outputting from the apparatus.

According to another broad aspect of the invention, a wake up circuit for initiating operation of a Manchester encoded data detector from a quiescent state in response to a Manchester data wake up sequence in an input signal is provided. The circuit includes a low pass filter circuit and hold circuit which is initially off to receive the input signal when the Manchester encoded data detector is in the quiescent state. The low pass filter circuit produces an output signal corresponding to the average value of the input signal. An offset circuit which is initially on shifts the low pass filter output signal to produce a voltage reference. A comparator circuit produces a data output signal corresponding to the difference between the voltage reference and the input signal. A circuit is provided for determining the time between transitions in ~~th~~ the comparator

output signal to selectively switch the hold circuit on after a first predetermined time, the hold circuit off and offset circuit on after a second longer predetermined time, and the hold circuit off immediately after any transition. A differential circuit produces an amplified input signal, and a circuit is provided for determining if a predetermined number of data cells have been sequentially received with respective predetermined states within the data output signal of the comparator circuit to selectively switch the offset circuit off.

The wake up circuit may also include a differential amplifier having inverting and noninverting inputs and an output. Also, the comparator circuit may include a first capacitor connected between the inverting input and a reference potential, and a second capacitor connected between the noninverting input and the reference potential. A first resistor may be connected between the input signal and the inverting input so that the voltage at the inverting input corresponds to the average value of the input signal.

The offset circuit may also include a first resistor connected between the inverting input of the differential amplifier and a voltage reference, a second resistor connected between the noninverting input and the input signal. A switch may be connected in series with the first resistor to turn the offset circuit on so that the voltage at the inverting input corresponds to the average value of the input signal plus an offset voltage. The output ~~of the output~~ of the differential amplifier produces the data output signal corresponding to the difference between the average value of the input signal pulse offset voltage and the input signal when the first switch is closed.

The comparator circuit may also include a second switch in series with the first resistor so that when the second switch is

closed and the first switch is opened, the output of the differential amplifier produces the amplified difference between the input signal and the average value of the input signal.

According to still another broad aspect of the invention, a method is provided for decoding Manchester encoded data to produce an nonreturn to zero binary representation of the data. The method includes producing a pulse for each transition of the Manchester encoded data, and generating a sampling signal in timed phase with the pulse for each transition of the Manchester encoded data. The Manchester encoded data is then latched at each occurrence of the sampling signal an output of the latched data is produced. An adaptive threshold detection is used to receive the Manchester encoded data with enhanced noise immunity. The step of using adaptive threshold detection, in one embodiment, includes providing a plurality of operating modes at a data input stage of a decoding circuit, such as a "steady-state" mode and "offset" mode of operation. In one embodiment, a "wake-up" mode of operation is provided.

According to yet another broad aspect of the invention, a timing recovery and Manchester data decoding system is presented. The system includes an oscillator providing output pulses and a multimode input circuit connected to receive a input signal that may contain a Manchester encoded data signal and to output a data containing signal. A transition detector is connected to receive the output signal from the multimode input circuit for generating a Manchester transition indicating pulse at every Manchester data transition. A counter synchronized by Manchester transitions circuit is connected to divide the output pulses from the oscillator by a predetermined count to produce output pulses starting a predetermined number of oscillator pulses after a Manchester data transition. A divide-by-2 circuit is connected to receive the pulses from the counter circuit to

generate a sample command signal, and a sampling circuit is connected to receive the output from the divide-by-2 circuit and the Manchester encoded data to latch the state of the Manchester encoded data in response to the output from the divide-by-2 circuit.

In one embodiment, the timing recovery and Manchester data decoding system may also include a mode decoder circuit, which may be a logic gate array or similar circuit, connected to receive the output count from the counter circuit to provide outputs on preselected counts of the output count from the counter circuit. Also, a mode control circuit may be connected to receive at least some of the outputs of the mode decoder circuit, the mode control circuit being connected to selectively control the mode of the multimode input circuit.

The timing recovery and Manchester data decoding system may also include an output control circuit connected to receive the data latched by the sampling circuit and the transition indicating pulses for producing an NRZ output data signal and output timing pulses, and, if desired, a circuit to delay the output timing pulses by one half cycle of the oscillator frequency.

The multimode input circuit in one embodiment has a "steady-state" mode in which a signal that contains a Manchester encoded data stream is processed and an output binary NRZ signal is produced at the output, an "offset" mode during which the occurrence of a wake up Manchester data sequence is needed to cause the circuit to "wake-up" to assume and resume the "steady-state" operating mode, and a "hold" mode during which circuit biases are maintained even though "steady-state" mode Manchester encoded data is not being received.

The multimode input circuit may include a comparator with inverting and non-inverting inputs, with a first resistor by

which the input signal is connected to the non-inverting input, and a second resistor by which the input signal is applied to the inverting input. A third resistor is connected at one end to the inverting input of the comparator. A first switch function is connected in series with the second resistor, and a second switch function is connected between another end of the third resistor and a reference voltage. A first capacitor is connected between the inverting input of the comparator and ground, and a second capacitor is connected between the non-inverting input of the comparator and ground. The first and second switch functions are controlled by the mode control circuit.

According to still another broad aspect of the invention, an apparatus for producing an NRZ data signal corresponding to second half states of Manchester cells in a Manchester data stream is provided. The apparatus includes an oscillator to produce a stream of clock pulses and a pulse generator connected to receive the Manchester data stream for generating an output pulse at each transition in the Manchester data stream. A divide-by-n counter is connected to be clocked by the clock pulses from the oscillator and reset by pulses from the pulse generator, the divide-by-n counter having an output that changes state after a predetermined number of the clock pulses. A timing flip-flop is connected to be clocked by the output from the divide-by-n counter, the flip-flop being connected to produce an output on every second count of the output from the divide-by-n counter. A sampling flip-flop is connected to receive the Manchester data stream on a data input and an output of the timing flip-flop on a clock input. The sampling flip-flop provides the then existing state of the Manchester data stream at an output when the sampling flip-flop is clocked. A sequence counter is connected to receive the output of the divide-by-n counter on a clock input and the output pulses from the pulse

generator on a reset input, whereby the sequence counter produces a signal indicating when a double wide Manchester pulse has occurred, the signal being connected to reset the timing flip-flop.

According to yet another broad aspect of the invention, a method for producing an NRZ data signal corresponding to states of a known half of each Manchester cell in a Manchester data stream is presented. The method includes the steps of generating a transition pulse at each transition in the Manchester data stream, and generating a series of timing pulses having a frequency n times a frequency of the Manchester cells in the Manchester data stream. The series of timing pulses is restarted in response to each transition pulse, and a current state of a Manchester cell is latched upon the occurrence of each m^{th} timing pulse, wherein m greater than n/2. The timing pulses are concurrently counted to provide a timing pulse count, the count being restarted in response to each transition pulse. If the timing pulse count becomes greater than n/2, the latching is advanced to latch the Manchester data stream upon the next $(n/2)^{th}$ occurring timing pulse.

In still yet another broad aspect of the invention, a method for producing an NRZ data signal corresponding to second half states of Manchester cells in a Manchester data stream is presented in which a series of timing pulses having a frequency twice the frequency of the Manchester cells in the Manchester data stream is generated. A current state of a Manchester cell is latched upon the occurrence of each second timing pulse. The occurrence of a double wide pulse in the Manchester data stream is detected, and the latching is resynchronized to begin on a next occurring timing pulse after the double wide pulse has been detected.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is illustrated in the accompanying drawings, in which:

FIGURE 1 shows a typical Manchester data stream and a nonreturn to zero data stream derived therefrom using the timing recovery and decoding system, in accordance with a preferred embodiment of the invention.

FIGURE 2 is an electrical block diagram of a general system for decoding Manchester data, illustrating, in conjunction with the various waveforms shown in FIGURE 3, the overall operation of the system and the mechanism for synchronizing the system to detect a predetermined half of each Manchester data cell, in accordance with a preferred embodiment of the invention.

FIGURE 3 shows a series of waveforms generated in the operation of the circuit of FIGURE 2, showing the manner by which the system automatically identifies the existence of valid Manchester data, and by which the system decodes it.

FIGURE 4 is an electrical block diagram of a system for decoding Manchester data similar to that of FIGURE 2, with additional short and long dead time detection features and with long term sleep and wake-up capabilities, in accordance with the invention.

FIGURE 5 is a more detailed electrical schematic block diagram showing a timing recovery and decoding system for Manchester encoded data or the like, in accordance with a preferred embodiment of the invention.

FIGURE 6 is an electrical schematic diagram of an oscillator for use in the timing recovery and decoding system of FIGURE 5.

FIGURE 7 is an electrical schematic diagram of a transition detector for use in the timing recovery and decoding system of FIGURE 5.

FIGURE 8 is an electrical schematic diagram of a transition counter for use in the timing recovery and decoding system of FIGURE 5.

FIGURE 9 is an electrical schematic diagram of a divide by two circuit for use in the timing recovery and decoding system of FIGURE 5.

FIGURE 10 is an electrical schematic diagram of a mode decoder circuit for use in the timing recovery and decoding system of FIGURE 5.

FIGURE 11 is an electrical schematic diagram of a pulse generator circuit for use in the timing recovery and decoding system of FIGURE 5.

FIGURE 12 is an electrical schematic diagram of a mode control circuit for use in the timing recovery and decoding system of FIGURE 5.

FIGURE 13 is an electrical schematic diagram of a transition counter circuit for use in the timing recovery and decoding system of FIGURE 5.

FIGURE 14 is an electrical schematic diagram of an output circuit for delivering an NRZ data output and accompanying timing or trigger pulses that have been derived from the input data stream that contains Manchester encoded data, for use in the timing recovery and decoding system of FIGURE 5.

FIGURE 15 is an electrical schematic diagram of a test mode select circuit for use in the timing recovery and decoding system of FIGURE 5.

FIGURES 16a-c are illustrative electrical waveforms showing the output signals from the threshold detector circuit of FIGURE 15 in each of the operating modes of the timing recovery and decoding system of FIGURE 5.

FIGURE 17 shows a waveform pulse series with a wake-up sequence and short dead time interval that may be employed in the circuit of the present invention.

FIGURE 18 is a series of detailed waveforms at various nodes of the input comparator circuit during a wake-up sequence, in accordance with one aspect of the present invention.

FIGURE 19 is an electrical schematic diagram of a threshold detector circuit, in greater detail, for use in the timing recovery and decoding system of FIGURE 1.

In the various figures of the drawings, like reference numerals are used to denote like or similar parts.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows an example of Manchester encoded data. The waveform 10 has a sequence of equal length data cells 12 - 22, with each cell representing a bit of corresponding binary data. There are transitions at the midpoint of every cell, which divide the Manchester data cells into two intervals or symbols. Positive going mid-cell transitions, such as the transitions 25, represent binary 1's; negative going mid-cell transitions, such as the transitions 26, represent binary 0's.

A constant series of 0's or a constant series of 1's produce identical square waves with pulse widths equal to a symbol time and periods equal to a cell time, such as the cells 12 - 15 or the cells 20 - 22. The waveforms differ only in phase. They cannot be distinguished without other information such as whether two adjacent symbols are in the same cell or are in adjacent cells, or, equivalently, whether a transition is at mid-cell or at a cell boundary.

In contrast to constant 1's or constant 0's, the Manchester representation of alternate 1's and 0's is not ambiguous. A "10" results in a two symbol wide Manchester high, such as represented by cells 16 and 17, and a "01" produces a two symbol

wide Manchester low, such as represented by cells 17 and 18. These double wide pulses always straddle a cell boundary, and thus provide a basis for orienting the timing reference, which is used in the implementation of one circuit embodiment of the present invention. Once the timing reference is established, single wide pulses representing constant data can be correctly decoded.

A general electrical block diagram of a system 400 for decoding Manchester data is shown in Figure 2, in which the overall operation of the system is illustrated in conjunction with the various waveforms shown in Figure 3. Timing for the system is provided by an oscillator 35, which produces a stream of clock pulses, labeled "SCLK," as seen in Figure 3. The Manchester data stream to be decoded, denoted MDAT, is brought into the system 400 on an input line 88, decoded data, denoted DOUT, is outputted from the system on line 255, and decoded timing, denoted TRIG, is outputted on line 259.

The Manchester data is initially connected to the input of a transition triggered one-shot pulse generator 45 (referred to herein as the transition detector 45), which generates a single output pulse at each positive or negative going data transition, the output pulses being denoted M2DAT on line 83. Representative waveforms for MDAT and M2DAT are shown in Figure 3. It can be observed from Figure 3 that MDAT is not necessarily synchronous with the clock pulses SCLK from the oscillator 35, but that a M2DAT pulse exists at each transition of MDAT.

The M2DAT output signal from the transition detector 45 on line 83 is connected to clear or reset a divide-by-5 counter 75, which is connected to be clocked by the clock pulses SCLK from the oscillator 35 on line 87. The divide-by-5 counter 75 has various separate outputs for each count, the output for count 3 (herein "the count-3 output") being connected to clock a D-type

flip-flop 105, and the output for count 4 being connected back to reset the transition detector 45. The output from the divide-by-5 counter 75 is a waveform, labeled 2XCK, having a frequency that is twice the expected frequency of the Manchester data signal MDAT.

In normal operation, the D-type flip-flop 105 clocks a sampling D-type flip-flop 120 at each second transition of the 2XCK signal, corresponding to the second half of the detected Manchester cell. Since the output of the divide-by-2 D-type flip-flop 105 is connected to clock the sampling D-type flip-flop 120, whenever the signal SSMS from the D-type flip-flop 105 changes state from negative to positive, the sampling D-type flip-flop 120 clocks the state of the then existing Manchester data on line 88 to the output, DOUT, on line 255. The sampling D-type flip-flop 120, therefore, produces an NRZ data output, DOUT, on line 255, replicating the state of the Manchester data from each successive time that the D-type flip-flop 120 is clocked.

It will be appreciated that if appropriate synchronizing precautions were not taken, it would be possible for the system to lock onto a data decoding sequence of 2XCK pulses that correspond to the timing of the first half of the Manchester data cells. Thus, the count-3 output from the divide-by-5 counter is also connected to clock a sequence counter 402. The sequence counter 402 operates to count a predetermined number of transitions of the 2XCK signal before being reset by the M2DAT signal on line 83. For example, in the embodiment illustrated, two transitions of the 2XCK signal are counted before the count-2 output of the sequence counter 402 produces a state change. Therefore, the output from the count-2 output of the sequence counter 402 provides a signal DB2INI on line 107 that indicates

the occurrence of a double wide pulse in the Manchester data, and serves to reset the divide-by-2 D-type flip-flop 105.

As mentioned, in the embodiment illustrated, the second half of the Manchester cell is desired to be sampled. Consequently, an orientation process is initiated by detecting when two consecutive 2XCK pulses occur during a single state of MDAT pulse (i.e., a state in which a midpoint transition is expected, but does not occur). More particularly, with reference to Figure 3, whenever two consecutive 2XCK pulses occur without an intermediate Manchester data state change, indicating a "double-wide" Manchester data pulse has occurred, such as the pulse 404 or the pulse 426, the output DB2INI on line 107 changes state to clear the D-type flip-flop 105 to synchronize the system to the second half of each Manchester data cell.

For example, the first MDAT pulse 404 shown is a "double-wide" pulse, produced, for instance, by a "01" or "10" value of the data represented by the Manchester signal to be decoded. The double-wide pulse produces transitions 406 and 407 in the M2DAT signal at its respective positive and negative going transitions. The first M2DAT pulse 406 resets the divide-by-5 counter, which proceeds to count clock pulses SCLK. It also resets the sequence counter 402. The output 2XCK on the count-3 output stays low, as shown by the signal segment 410, until three clock pulses have occurred, at which time the count-3 output is set. The count-3 output stays high for two additional counts, shown by the pulse segment 411, until the divide-by-5 counter reaches the count of 5.

At that time, since no state change has occurred in the Manchester data pulse 404, no transition detecting pulse was generated in the M2DAT stream, so the divide-by-5 counter proceeds to immediately count a new data sequence. After the second count of 3, the output of the divide-by-5 counter changes

state, shown by the 2XCK data stream segments 414 and 416. Additionally, since the sequence counter 402 was not reset, due to the absence of an MDAT transition, when the second consecutive 2XCK pulse 416 occurs, a synchronizing pulse DB2INI is generated. It can be seen that following a double-wide Manchester pulse, the next occurring state change will be a proper midpoint transition. Thus, when the DB2INI pulse resets the divide-by-2 D-type flip-flop 105, upon the occurrence of the next occurring 2XCK signal, the divide-by-2 D-type flip-flop 105 generates an SSMS signal, assured to be in the second half of the Manchester cell, to clock the sampling D-type flip-flop 120, thereby synchronizing the system to sample the second halves of subsequently occurring Manchester data cells.

Still more particularly, as shown, following the Manchester data pulse segment 404 the Manchester data signal experiences a midpoint transition to segment 426 prior to the next count of 3 SCLK pulses in segment 418 of the 2XCK signal. This causes a transition indicating M2DAT pulse 407 to be generated, which resets the divide-by-5 counter and starts a new count. The next occurring 2XCK pulse 419, which occurs in the second half of the Manchester data cell timing, clocks the D-type flip-flop 105, which in turn clocks the sampling D-type flip-flop 120, which samples and latches the Manchester data existing at that time.

It should be appreciated that although the timing of the 2XCK pulses have been described as being twice that of the Manchester data cells, any multiple, n, may be selected, with appropriate adjustment to the dividers to select the particular 2XCK pulse that occurs during a second half of each Manchester cell. The resetting adjustment provided by the sequence counter may be also changed to reset the output latch to select an appropriate number of pulses by which to activate the latching function, for example, n/2.

At the same time as the data is generated on output line 255, trigger pulses that are synchronized with the clock pulses SCLK on line 87 are generated on the output line 257, labeled TRIG. The relationship of each TRIG pulse to the rising edges of the pulses SSMS can be seen in Figure 3.

An electrical block diagram of a system 430 for decoding Manchester data similar to that described above with reference to Figure 2 is shown in Figure 4 to which reference now is made. The system 430 shown in Figure 4 has additional short and long dead time detection features and long term sleep and wake-up capabilities provided by a short dead time register 431 and long time register 432. The short and long dead time registers serve to adjust the thresholds of the input Manchester data conditioning circuit 41 and to disable the outputs of the system 430 when no Manchester data is detected for a predetermined length of time. The operation of the short and long dead time features of the system 430 are described below in detail.

Additionally, the system 430 of Figure 4 includes a sleep and wake-up feature provided by the long dead time register and a separate wake-up counter 165. The operation of the sleep and wake-up feature are also described below in detail.

Referring now to FIGURE 5, a more detailed block diagram of a timing recovery and Manchester data decoding system 34 is shown, in accordance with a preferred embodiment of the invention. A 50 kHz free running oscillator 35 provides the basic timing reference to the remainder of the circuitry. The oscillator 35 may be of standard construction, details of one embodiment of which being shown in Figure 6. Although the oscillator 35 is shown constructed of discrete logic components, such as the cross-coupled NAND gates 39 shown, the oscillator function can be provided by well known SAW devices, or other suitable oscillator devices or circuits (not shown).

With reference again to Figure 5, the input signal, which may contain a Manchester data encoded data stream to be decoded, is connected on an input line 40 to a multimode input circuit 41, which provides its output (MDAT) on line 42 to a transition detector 45. (In the embodiment illustrated, a test mode control circuit 55 is provided, below described in detail, which controls whether the input signal or a test signal is applied to the remaining portion of the timing recovery and Manchester data decoding system 34. The output from the test mode control circuit 55 is then delivered to the transition detector 45.)

The multimode input circuit 41 has a comparator 46 with inverting and non-inverting inputs as shown. The input signal is connected to the non-inverting input by a first resistor 47, and to the inverting input by a second resistor 48. A first switch 50, connected in series with the resistor 48, is controlled by a mode control circuit 160, below described in detail. Although the first switch 50 may be provided by a physical switch, or a transistor connected in known switch-function configuration, it will be appreciated that the purpose is to selectively apply the input signal to the inverting input of the comparator 46. Accordingly, equivalent circuitry may be employed to perform this selective voltage application, one example of which being the transfer gate 283 shown, for example, in one implementation of the multimode input circuit 41, shown in Figure 19.

A third resistor 56 is connected between the inverting input of the comparator 46 and a second switch 58, which also is controlled by the mode control circuit 160. The switch 58 is connected to a reference voltage, such as V_{cc}, shown. Again, the second switch 58 may be provided by a physical switch, or a transistor connected in known switch-function configuration; however, it will be appreciated that the purpose is to

selectively connect the voltage V_{cc} to the inverting input of the comparator 46. Accordingly, equivalent circuitry may be employed to perform this selective voltage application, one example of which being the current source 280 and mirror circuit 281 shown, for example, in the implementation of the multimode input circuit 41 in Figure 19. Two capacitors 60 and 61 are connected respectively between the inverting and non-inverting inputs of the comparator 46, and between the non-inverting input and ground.

The transition detector 45, which generates a positive Manchester transition indicating pulse (M2DAT) at every transition, positive or negative, of Manchester data, receives the output on line 42 from the multimode input circuit 41 on the input of a D-type flip-flop 64, shown in Figure 7. Clock pulses on line 87 from the oscillator 35 clock the D-type flip-flop 64, the output of which is connected to one input of an exclusive OR gate 65. The output of the exclusive OR gate 65 is connected to one input of a NAND gate 66, the output of which is connected to one input of a flip-flop 67 that includes NAND gates 68 and 69.

Another input of the flip-flop 67 receives a signal on line 71 from a counter 75, below described in detail, to insure that the transition detector 45 does not respond to the second of two transitions that are separated by a time less than a predetermined number of clock pulses, for instance, less than about 60 to 80 microseconds. The output of the flip-flop 67 is connected to the second input to the NAND gate 66 via inverters 77 and 78 and resistor 79. A capacitor 81 is connected between the input of the inverter 78 and ground to provide a low pass filter in conjunction with the resistor 79.

The output from the NAND gate 66 is connected to an inverter 84, which operates to produce a positive pulse (M2DAT),

for example of about 12 nanoseconds long, on the output line 83 whenever either a positive or negative transition occurs on the input line 42. An inverted output occurs on line 85, labeled "M2DATZ". Either the first or the second Manchester symbol may be selected by a Manchester transition counter 75, described below, which is clocked by the oscillator 35, and reset upon the occurrence of a Manchester data transition on line 85, as indicated by the Manchester transition indicating pulse (M2DAT).

Details of a suitable Manchester transition counter circuit 75 are shown in Figure 8, in which the clock pulses from the oscillator 35 are received on input line 87 and the output from the transition detector circuit 45 are received on input line 85. The Manchester transition counter 75 has three D-type flip-flops 90, 91, and 92 connected to receive the clock pulses on line 87 on their respective clock inputs and the Manchester transition signal on their clear or reset inputs. The output from the first D-type flip-flop 90 is connected to the data input of the second D-type flip-flop 91, and the outputs of the second and third D-type flip-flops 91 and 92 are connected to the input of the first D-type flip-flop 90 by a NOR gate 94. In addition, the output of the second and third D-type flip-flops 91 and 92 are connected to the inputs of a NAND gate 96, the output of the second D-type flip-flop 91 being inverted by an inverter 98.

The Manchester transition counter 75 operates as a modulo 5 clock pulse counter, with the divided clock pulses on output line 100 occurring after three counts produced by the oscillator 35 on line 87, after the counter 35 has been reset by the occurrence of a Manchester data transition on line 85. If no Manchester data transition resetting event occurs, the divided clock pulses on output line 100 are merely the clock frequency divided by five. The signal on output line 71 occurs after every

four counts following a Manchester data transition resetting event occurring on line 85, and is connected back to the input of the flip-flop 68 of the transition detector 45, described above.

It should be noted that the particular circuit embodiment of the present invention herein described decodes the Manchester data by sampling and latching the second symbol of each Manchester data cell, as determined by the delay count developed by the Manchester transition counter 75. It will be appreciated that the first symbol of the Manchester data could also be sampled, latched, and decoded by selecting a different delay count, then inverting the data.

The divided clock pulses from the counter 75 on output line 100 is connected to an input of a divide-by-2 circuit 105, details of which being shown in Figure 9. The divide-by-2 circuit 105 has a D-type flip-flop 106 that receives the divided clock pulses from the counter 75 on line 100 on its clock terminal. The reset line is connected to receive a reset signal from a mode decoder circuit 110, below described in detail. The output of the D-type flip-flop 106 is inverted by a NAND gate 112, and connected to the input. The other side of the NAND gate 112 is connected to receive a signal on line 113 from the mode decoder circuit 110, which indicates that there have been no Manchester data transitions for three consecutive periods of the divided clock pulses on line 100. The signal on line 113 is inverted by an inverter 114.

In operation, the divide-by-2 circuit 105 divides the divided clock pulses on line 100 by two, to generate a sample command signal on output line 117. As will become apparent, a reset signal will be generated on line 107 when two positive edges of the divided clock pulses on line 100 have occurred between any two successive Manchester data transition indicating

pulses on line 85. Since a transition must occur between the symbols of each Manchester cell, if two counts of the divided clock pulses on line 100 have occurred between Manchester data transitions, a reset signal generated by the second count insures that the circuit is synchronized to the correct symbol of the Manchester cells, and a double-wide pulse has occurred (compare, for example, the double-wide pulses 27 in Figure 1). The double wide pulses always overlap the leading edges of two of the divided clock signal pulses on line 100, whereas single wide pulses always overlap only one. Since the reset signal on line 107 resets the D-type flip-flop 106, the operation of the divide-by-2 circuit 105 automatically synchronizes the circuit to detect the correct Manchester symbol upon the occurrence of the next count pulse of the divided clock pulses on line 100, and with every other one thereafter.

After the D-type flip-flop 106 has been reset, the next positive edge of the divided clock pulses on line 100 causes the sample command signal on line 117 to go high, actuating the sample block 120 (below described) to sample the received Manchester data during the second Manchester data symbols. If there are no Manchester data transitions for three consecutive periods of the divided clock pulses on line 100, the signal delivered on line 113 goes high, forcing the output of the NAND gate 112 high. This causes the sample command signal on line 117 to go high upon the occurrence of the next positive edge of the divided clock pulses on line 100. When the Manchester data transitions begin again, the D-type flip-flop 106 is set up to sample the second half of the Manchester cell, since the first positive edge of the divided clock pulses on line 100 will clock the sample command signal on line 117 to its low state. The next positive edge of the divided clock pulses on line 100 clocks the

output to a high state, which causes the sample circuit 120 to sample the current Manchester data.

The sampling circuit 120, as shown in Figure 5, is a D-type flip-flop 121 in the embodiment illustrated. The signal that contains the Manchester data (MDAT) is connected to the data input, and the output is connected to an output control circuit 125, below described. By clocking the D-type flip-flop 121 with sampling pulses of the frequency and phase of the second symbol of each Manchester data cell, the sampling flip-flop 121 correctly samples and latches the Manchester data signal on line 250. At this point it should be noted that since the logic level of the latched Manchester data is constant between samples, the resulting data is a binary nonreturn-to-zero (BNRZ) binary representation of the encoded data, shown by waveform 30 in Figure 1.

As discussed above, selecting every other divided clock pulse on line 100 provides the correct frequency for the sampling pulse waveform. However, without initialization, there is an equally likely possibility that the sampling pulses will align with the first symbol rather than the second, and the decoded data would be inverted. The proper alignment is determined by the mode decoder circuit 110, which detects the existence of a double wide Manchester waveform. Details of the mode decoder circuit 110 are shown in Figure 10.

In general, the mode decoder circuit 110 decodes counts from the pulse generator circuit 130, below described in detail, and is essentially a logic gate array that provide outputs on output lines 132-136 and 107 of known logic states for various input count combinations. The circuit has four input NAND gates 140-143, which receive the outputs on lines 180 - 188 from the pulse generator circuit 130.

The NAND gates 140 and 141 receive their inputs on lines 181-185 from the pulse generator circuit 130. The outputs from NAND gates 140 and 141 are connected to the inputs of a NOR gate 150, which produces an output on line 132 that goes high on count number 63 of the divided clock pulses on line 100, when all of the count signals on lines 180-185 are high. The signal on output line 132 serves to inhibit the input to the pulse generator circuit 130, as below described.

The NOR gate 153 receives the outputs from the NAND gates 142 and 143, as well as an input on line 185 to produce an output on line 154, indicating a count of three of the divided clock pulses on line 100. The line 154 is connected to both inputs of a NAND gate 155, which acts as an inverter, and to one input of a flip-flop 161, defined by NOR gates 156 and 157, to set the flip-flop when the third count has occurred. The output from the NAND gate 155 on line 133 goes low upon the count of three of the divided clock pulses on line 100, and is used to clear the transition counter circuit 165, as below described. Concurrently, the output from the flip-flop on line 134 goes high on the count of three of the divided clock pulses on line 100, and serves to enable the NAND gate of the divide-by-2 circuit 105 (Figure 9), as described above.

The other input to the flip-flop comprised of the NOR gates 156 and 157 is connected to receive the signal on line 83 from the transition detector 45 (Figure 7), indicating the occurrence of a Manchester data transition. When a signal is received indicating that a Manchester data transition has occurred, the flip-flop is reset, returning the output state on line 133 to a high state and the output state on line 134 to a low state.

The output from NAND gate 143, as well as the signal on line 185, are connected to the inputs of NOR gate 159. The output from the NOR gate 159, as well as the signal on line 181,

are connected to the inputs of a NAND gate 162, which produces an output on line 107 that goes low on the count of two of the divided clock pulses on line 100. The signal on the line 107 serves to reset the D-type flip-flop 106 of the divide-by-2 circuit 105 of Figure 9. The output signal from the transition counter 165, below described in detail, on line 166 is inverted by an inverter 167, and produced on the output line 136 to reset the D-type flip-flop 135 of the mode control circuit 160, below described.

The pulse generator circuit 130 that provides counts of the divided clock pulses on line 100 to the mode decoder circuit 110 is shown in detail in Figure 11. The pulse generator circuit 130 includes six D-type flip-flops 170-175, connected as a ripple counter. The divided clock pulses on line 100 and the signal indicating that the count has reached 63 on line 132 (from the NAND gate 150 of the mode decoder circuit 110, shown in Figure 10) are applied to the inputs of an OR gate 177. The counter is reset by the occurrence of a Manchester data transition indicating signal on line 85, and is clocked by the divided clock pulses on line 100, which is enabled by the OR gate 177. The outputs are developed on lines 180-188 and delivered to the mode decoder circuit 110, described above.

The operation of the pulse generator circuit 130 is to count the number of divided clock pulses on line 100 that occur between pulses that indicate transitions of the Manchester data appearing on line 85. The occurrence of a Manchester data transition indicating pulse on line 85 presets the counter to an all "ones" initial state, after which the divided clock pulses on line 100 are sequentially counted. If a count of ~~64~~ is reached, the signal from the mode decoder circuit 110 on line 132 goes high, inhibiting further clocking until the next Manchester data transition indicating pulse occurs.

Additional control signals are generated by the mode control circuit 160, details of which are shown in Figure 12. The mode control circuit 160 includes a D-type flip-flop 135 connected to receive the output on line 132 from the mode decoder circuit 110 of Figure 13. The output on line 132 indicates that the count of the divided clock pulses on line 100 has reached ~~64~~ 63. The D-type flip-flop 135 is connected to be reset by the output on line 136 from the mode decoder circuit 110 of Figure 13, which represents the inverted output on line 166 from transition counter 165, below described. The D-type flip-flop 135 is connected to be clocked by the divided clock pulses on line 100, connected via the OR gate 235. The output from the D-type flip-flop 135 is connected to a second input of the OR gate 235 to inhibit the divided clock pulses on line 100 when the output is high.

The inverted output from the D-type flip-flop 135 is connected to one input of a NAND gate 236, the output of which is an output signal on line 238 that is used to control the switch 50 of the input stage 41. The switch 50 also controls the operating mode of the circuit 34. The other input of the NAND gate 236 is connected to receive the output on line 134 from the mode decoder circuit 110, shown in Figure 10. The signal on line 134 goes high after the occurrence of the third count of the divided clock pulses on line 100.

The inverted output of the D-type flip-flop 135 is connected to set a flip-flop comprised of NAND gates 240 and 241. The flip-flop is reset by the signal on line 187 from the pulse generator circuit 130, corresponding to a count of eight divided clock pulses on output line 100. The output from the flip-flop is connected to one input of a NOR gate 242, which is connected to receive the signal on line 134 at its other input.

The output enable signal on line 244 is connected to enable the output control circuit 125, below described. Thus, in operation, the mode control circuit 160 prevents the output enable signal on line 244 from going high and enabling the outputs of the output control circuit 125 until after a short dead time of eight counts of the divided clock pulses on line 100.

The transition counter circuit 165 mentioned above in conjunction with the description of the mode decoder circuit 110, is shown in Figure 13, and has three D-type flip-flops 190-192. The first D-type flip-flop 190 is clocked by a change in state of the latched Manchester data appearing on line 250 at the output of the sample flip-flop circuit 120, provided the signal ~~LDT.B~~ LDT_B from the mode control circuit 160 remains low. When ~~LDT.B~~ LDT_B goes high, the OR gate 195 is inhibited from passing further transition signals. The output of the first D-type flip-flop 190 is connected to the clock input of the second D-type flip-flop 191, as well as to a first input of a three input NOR gate 196. The inverted output of the first D-type flip-flop 190 is connected to its data input.

The second D-type flip-flop 192 is similarly connected, with its inverted output connected to its input, and its output connected to the second input of the NOR gate 196 and to the clock input of the third D-type flip-flop 192. In a similar fashion, the third D-type flip-flop 192 is connected with its inverted output connected to its input; however, the inverted output is also connected to the third input of the three input NOR gate 196.

The three D-type flip-flops 190-192 are reset by the signal produced on output line 133 from the mode decoder circuit 110 (Figure 10), which goes low on the third count of the divided clock pulses on line 100, described above. Thus, the transition

counter 165 serves to count four positive edges of the sampled Manchester data, and operates to "wake up" the circuit after a long dead time period. Although the wake up features of the circuit are described below in detail, briefly, if a count of four is reached before the resetting signal occurs on line 133, the output on line 166 goes high, waking up the remainder of the circuit in the manner below described.

The input BNRZ on line 250 to the transition counter circuit is also applied to the output control circuit 125, details of which are shown in Figure 14. The output control circuit 125 receives the decoded BNRZ signal from the sampling or latching flip-flop 121 into an enabling AND gate 252, which has an output that is buffered by an output buffer 253 to provide a data out signal (DOUT) on the data out line 255. The AND gate 252 is enabled by the output enable signal, which is developed on line 244 from the output of the NOR gate 242 of the mode control circuit 160, described above with reference to Figure 12.

The trigger or timing output (TRIG) on line 257 is developed by an enabled AND gate 260, the output of which is buffered by the output buffer 261. The AND gate 260 also is enabled by the output enable signal on line 244 from the NOR gate 242 of the mode control circuit 160. The other input to the AND gate 260 is derived from the clock signal from the oscillator 35, developed on line 87, delayed by one-half cycle. The clock signal on line 87 is inverted by inverter 265 to clock the sample command signal on line 117, developed by the divide-by-2 counter 105 described above with reference to Figure 9, into a D-type flip-flop 268.

The one-half cycle delay of the clock pulses on line 87 is produced by the D-type flip-flop 270, which receives the output from the D-type flip-flop 268 on its data input and the clock

pulses on line 87 on its clock input. The output from the D-type flip-flop 270 is connected to one input of a NOR gate 271, the output of which is connected to the AND gate 260. The other input to the NOR gate 271 is the output from the D-type flip-flop 268, which is inverted by an inverter 272.

The timing pulses developed on output line 257 are delayed from a state change of the sample command signal on line 117 at the output of the divide-by-2 counter 105 (and therefore the binary NRZ signal on line 250) by half a period of the clock signal on line 87. The delay may be, for example, on the order of about 10 μsec. The output timing pulse is then one-half period of the clock signal on line 87, also about 10 μsec.

The waveforms on the data out line 255 and timing signal output line 257 are copies of the BNRZ (binary nonreturn to zero) output of the sampling flip-flop 120 and the sampling pulses at the output from the output of the divide-by-2 circuit 105, except that the timing signal output on line 257 is delayed one half period of the period of the divided clock pulses on line 100.

In contrast to normal circuit operation, described below, the timing recovery and Manchester data decoding system 34 provides for a test mode, in which a test signal can be applied to the circuit via a test mode control circuit 55, shown in Figure 15. Thus, the circuit 34 normally receives the Manchester data containing signal (MDAT) at its the multimode input stage 41 under the control of the mode control circuit 160, details of which are shown in Figure 12. However, in order to provide a test mode of operation, with reference again to Figure 15, the output from the multimode input stage 41 is connected on line 42 to the inputs of a NAND gate 210, a NOR gate 211, and a multiplexer circuit 212. The outputs from the NAND gate 210 and

NOR gate 211 are inverted respectively by inverters 214 and 215, and may be used for desired test or monitoring purposes.

The multiplexer circuit 212 normally produces the Manchester data containing signal on line 42 at its output on line 88 to the remaining circuitry, as discussed above. However, if a high test enable signal is applied to the test enable line 220, a Manchester data containing test signal that is applied on the line 221 is delivered to the output line 88.

As indicated above, the timing recovery and Manchester data decoding system 34 has three operating modes, depending upon the conditions established by the Manchester data contained in the input signal. The three operating modes provide for an adaptive threshold detection scheme of operation, depending upon the character and nature of the input signal. The first operating mode is the "steady-state" mode, as described above, in which a signal that contains a Manchester encoded data stream is processed and an output binary NRZ signal is produced at the output. The second operating mode is an "offset" mode in which the circuit 34 is "sleeping," during which the occurrence of a wake up Manchester data sequence is needed to cause the circuit to "wake-up" to assume and resume the "steady-state" operating mode. The third operating mode is a "hold" mode in which the circuit operates between the detection of the wake up sequence and reception of normal data, during which the circuit biases are maintained, even though steady-state mode Manchester encoded data is not being received.

The particular mode in which the circuit operates depends upon how the comparator 46 is biased by the switches 50 and 58. Thus, the switches 50 and 58 are operated to select one of three reference voltage settings, based on signal conditions detected from monitoring the Manchester transition indication waveform in

response to the signals on line 238 of the mode control circuit 160 shown in Figure 12.

The waveforms produced for the three reference voltage settings are outlined in Figures 16a-c. With reference also again to Figure 5, as is apparent the time constant at node 2 at the inverting input of the comparator 46 is much greater than at node 1 at the noninverting input of the comparator 46. Consequently, node 2 responds primarily to the long term average of the DASK (Demodulated ASK) signal whereas node 1 responds to DASK data transitions. In the "steady-state" mode of operation, having waveforms shown in Figure 16a, switch 50 is closed and switch 58 is open. In the "steady-state" mode, the reference voltage 300 at node 2 will equal the average value of the signal 302 at node 1. Since the average value of the Manchester data is always centered between the high and low levels, maximum noise immunity is achieved.

In the "hold" mode, having waveforms shown in Figure 16b, both switches 50 and 58 are open. Since there is no discharge path, the capacitor 60 on node 2 holds the previous voltage, seen as waveform 304. For transmission formats that contain bursts of data separated by short dead time intervals, such as represented by waveform 306, the "hold" mode retains the optimum threshold between bursts of valid data.

In the "offset" mode, having waveforms shown in Figure 13c, the reference voltage 308 at node 2 is offset from the average value of the noise at node 1. The offset voltage is chosen so that the reference is approximately at the midpoint of the high and low levels of the weakest valid signal 310 expected at node 1. This mode is used during long dead time intervals. Comparator output noise is suppressed far below that which is seen in most remote control receivers where the reference voltage is allowed to become equal to the noise average value.

Although the comparator noise immunity in the "offset" mode may not be as good as in the "steady-state" mode, a simple transmission format combined with further signal processing can nearly eliminate the possibility of a false wake-up sequence followed by noise at the data out line 255 (Figure 14). A format with a wake-up sequence and short dead time interval such as shown in Figure 17 may be used. As can be seen, the wake-up sequence includes a number of similar pulse transitions 314-323, followed by a dead time interval 326, which, in turn is followed by the desired Manchester data stream 328,330. In the embodiment illustrated, an initial sequence of 8 Manchester transitions 328 is sent to assure proper synchronization, although this is not absolutely necessary. After the synchronizing sequence 328, the actual Manchester data of interest 330 is transmitted. With this format, the data out on line 255 and the timing pulses on output line 257 from the output control circuit 125 (Figure 14) are only active after a valid wake-up sequence and short dead time have occurred. They will remain active until another dead time interval is detected.

The mode control circuit 160 responds to the Manchester transition indicating pulse and divided clock pulses on line 100 to determine the appropriate comparator reference mode. During a long dead time, the "offset" mode is in effect, and any detected transitions of the transition indicating pulse starts a candidate wake up sequence. The comparator 46 remains in the "offset" mode until a valid wake up is detected. A valid wake up consists of a predetermined number of properly spaced sequential transitions. For proper spacing, the separation between any two transitions must be less than three symbol widths. This is determined by counting the divided clock pulses on line 100 following every transition. If the count reaches three, the

sequence is rejected and starts over at the next detected transition.

More particularly, as shown in Figure 18, the waveforms at various nodes of the input circuit 41 are shown in greater detail. During a wake up sequence, the reference for the comparator 46 charges toward a final value of the signal average plus offset, shown by curve segment 340. Following wake up, the reference is switched to "normal" mode at point 342. As is apparent from the figure, during wake up the reference charges more quickly toward the average value than it would if "steady-state" mode were used. This is due to both the reduced time constant and the presence of an offset voltage. Since in the embodiment illustrated there are twelve transitions in the wake up burst, but only four are required for wake up, the system will ordinarily be awake before the entire burst is complete. Although this allows additional time for the reference to settle toward the true average value, it is obviously advantageous if it is already close when "steady-state" mode is switched in. This is particularly true for very weak signals or high noise conditions where wake up can occur near or at the end of the wake up burst.

After the circuit has been awakened, a short dead time occurs in region 344. (It should be noted that the dead time region 344 illustrated in Figure 18 has been shortened for purposes of illustration. A typical dead time may be, for example on the order of 2 milliseconds, or longer.) The data out signal on line 255 and the timing pulses on line 257 are enabled at the end of the short dead time that follows wake up. This hold off prevents outputting data from the remaining portion of the wake up burst. The short dead time is detected by counting the divided pulses on line 100 following each Manchester transition pulse. If the count reaches three, a short dead time

is initiated and the comparator reference is switched to hold mode. These settings remain in effect until either detected transitions resume or the count of divided clock pulses on output line 100 reaches 64. If detected transitions occur first, the count of the divided clock pulses on output line 100 is set to zero, the comparator reference is set to the "steady-state" mode, the outputs are enabled, and decoded data and timing pulses or triggers appear at respective output lines 255 and 257.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the spirit and scope of the invention, as hereinafter claimed.

CLAIMS:

1. An apparatus for decoding a Manchester encoded data stream, comprising:

a transition detector for receiving the Manchester encoded data stream to produce a transition indicating output when a transition of the Manchester encoded data stream is detected;

a circuit to generate an output control pulse a predetermined time after said transition indicating output is produced;

a sampling flip-flop receiving the Manchester encoded data stream, controlled by the output control pulse to output a state of the Manchester encoded data when said output control pulse is generated.

2. The apparatus of claim 1 wherein said sampling flip-flop operates to generate a binary NRZ form of the Manchester encoded data stream.

3. The apparatus of claim 1 further comprising a clock generator for generating a clock pulse stream at a frequency higher than said Manchester encoded data stream.

4. The apparatus of claim 3 wherein said transition detector is connected to receive said clock pulse stream and is configured to synchronize the transition indicating output with a pulse of said clock pulse stream.

5. The apparatus of claim 1 further comprising a phase selector to select a known half of a Manchester data cell occurring after a transition.

6. The apparatus of claim 5 wherein said phase selector selects a second half of a Manchester data cell.

7. The apparatus of claim 5 wherein said phase selector selects a first half of a Manchester data cell.

8. The apparatus of claim 7 further comprising an inverter to invert the output from said flip-flop.

9. A timing recovery and Manchester data decoding system, comprising:

an oscillator providing output pulses;

a multimode input circuit connected to receive an input signal that may contain a Manchester encoded data signal and to output a data containing signal;

a transition detector connected to receive the output signal from the multimode input circuit for generating a Manchester transition indicating pulse at every Manchester data transition;

a Manchester transition counter circuit connected to receive the output pulses from the oscillator to produce a predetermined number of oscillator pulses after a Manchester data transition;

a divide-by-2 circuit connected to receive the oscillator pulses from the Manchester transition counter circuit to generate a sample command signal;

and a sampling circuit connected to receive the output from the divide-by-2 circuit and the Manchester encoded data to latch the a state of the Manchester encoded data in response to the output from the divide-by-2 circuit.

10. The timing recovery and Manchester data decoding system of claim 9 further comprising:

a pulse generator circuit connected to receive output pulses from said oscillator and produce an output count thereof;

a mode decoder circuit connected to receive the output count from said pulse generator circuit to provide outputs on preselected counts of said output count from said pulse generator circuit;

and a mode control circuit connected to receive at least some of the outputs of said mode decoder circuit, said mode control circuit being connected to selectively control the mode of said multimode input circuit.

11. The timing recovery and Manchester data decoding system of claim 10 wherein said mode decoder circuit is a logic gate array.

12. The timing recovery and Manchester data decoding system of claim 9 further comprising:

an output control circuit connected to receive the data latched by said sampling circuit and said transition indicating pulses for producing an NRZ output data signal and output timing pulses.

13. The timing recovery and Manchester data decoding system of claim 12 further comprising a circuit to delay the output timing pulses by one half cycle.

14. The timing recovery and Manchester data decoding system of claim 9 wherein said multimode input circuit has a "steady-state" mode in which a signal that contains a Manchester encoded data stream is processed and an output binary NRZ signal is produced at the output, an "offset" mode during which the occurrence of a wake up Manchester data sequence is needed to

cause the circuit to "wake-up" to assume and resume the "steady-state" operating mode, and a "hold" mode during which circuit biases are maintained even though "steady-state" mode Manchester encoded data is not being received.

15. The timing recovery and Manchester data decoding system of claim 9 further comprising a test mode control circuit for controlling whether the input signal or a test signal is processed.

16. The timing recovery and Manchester data decoding system of claim 9 wherein said multimode input circuit comprises:

a comparator with inverting and non-inverting inputs;

a first resistor by which the input signal is connected to the non-inverting input;

a second resistor by which the input signal is applied connected to the inverting input;

a first switch function in series with the second resistor;

a third resistor connected at one end to the inverting input of the comparator;

a second switch function connected between another end of said third resistor and a reference voltage;

a first capacitor connected between the inverting and non-inverting input of the comparator;

and a second capacitor connected between the non-inverting input of the comparator and ground;

said first and second switch functions being controlled by said mode control circuit.

17. A wake up circuit for initiating operation of a Manchester encoded data detector from a quiescent state in response to a Manchester data wake up sequence in an input signal; comprising:

an input circuit with a hold mode which is initially off to receive the input signal when the Manchester encoded data detector is in the quiescent state to produce a data output signal corresponding to a sampled state of the input signal;

an offset circuit which is initially on to receive the input signal to compare the input signal to a voltage reference derived from an input signal average value plus a predetermined offset voltage to produce a data output signal corresponding to the difference between the voltage reference and the input signal;

a circuit for determining if a possible Manchester encoded data cell has been received in the data output signal from the sample and hold circuit to selectively switch said offset circuit on;

and a circuit for determining if a predetermined number of data cells have been sequentially received with respective predetermined states within said data output signal of said offset circuit to selectively switch said offset circuit off.

18. The wake up circuit of claim 17 further comprising a differential amplifier having inverting and noninverting inputs and an output, and wherein:

said input circuit comprises a first capacitor connected between said inverting input and a reference potential, and a second capacitor connected between said noninverting input and said reference potential, and a first resistor connected between said input signal and said inverting input, wherein said data output signal is produced at the output of said differential amplifier;

said offset circuit comprises a first resistor connected between said inverting input of said differential amplifier and said voltage reference, a second resistor connected between said inverting input and said input signal, and a switch connected in series with said second resistor to turn said offset circuit on, wherein said output of said differential amplifier produces said data output signal corresponding to the difference between the voltage reference and the input signal when said first switch is closed; and

said differential circuit comprises a second switch in series with said second resistor, wherein when said second switch is closed and said first switched is opened, said output of said differential amplifier produces said amplified input signal.

19. A method for decoding Manchester encoded data to produce an nonreturn to zero binary representation of the data, comprising:

producing a pulse for each transition of the Manchester encoded data;

generating a sampling signal in timed phase with the pulse for each transition of the Manchester encoded data;

latching the Manchester encoded data at each occurrence of the sampling signal and producing an output of the latched data;

and using adaptive threshold detection to receive the Manchester encoded data with enhanced noise immunity.

20. The method of claim 19 wherein said step of using adaptive threshold detection comprises providing a plurality of operating modes at a data input stage of a decoding circuit.

21. The method of claim 20 wherein said step of providing a plurality of operating modes comprises providing steady-state" and "offset" modes of operation.

22. A method for producing an NRZ data signal corresponding to states of a known half of each Manchester cell in a Manchester data stream, comprising:

generating a transition pulse at each transition in the Manchester data stream;

generating a series of timing pulses having a frequency n times a frequency of said Manchester cells in said Manchester data stream;

restarting said series of timing pulses in response to each transition pulse;

latching a current state of a Manchester cell upon the occurrence of each m^{th} timing pulse, wherein m greater than n/2;

counting said timing pulses to provide a timing pulse count;

restarting said counting in response to each transition pulse; and

if said timing pulse count becomes greater than n/2, advancing said latching to latch said Manchester data stream upon the next $(n/2)^{th}$ occurring timing pulse.

23. The method of claim 22 wherein said multiple of the frequency of said timing pulses is twice the frequency of said Manchester data stream, and wherein n is 2.

24. A method for producing an NRZ data signal corresponding to second half states of Manchester cells in a Manchester data stream, comprising:

generating series of timing pulses having a frequency half of a frequency of said Manchester cells in said Manchester data stream;

latching a current state of a Manchester cell upon the occurrence of each second timing pulse;

detecting the occurrence of a double wide pulse in said Manchester data stream;

and resynchronizing said latching to begin on a next occurring timing pulse after said double wide pulse has been detected.

25. Apparatus for producing an NRZ data signal corresponding to second half states of Manchester cells in a Manchester data stream, comprising:

an oscillator to produce a stream of clock pulses;

a pulse generator connected to receive said Manchester data stream for generating an output pulse at each transition in said Manchester data stream;

a divide-by-n counter connected to be clocked by said clock pulses from said oscillator, said divide-by-n counter having an output that changes state after a predetermined number of said clock pulses;

a timing flip-flop connected to be clocked by said output from said divide-by-n counter, said flip-flop being connected to produce an output on every second count of said output from said divide-by-n counter;

a sampling flip-flop connected to receive said Manchester data stream on a data input and an output of said timing flip-flop on a clock input, said sampling flip-flop providing a state of said Manchester data stream at an output when said sampling flip-flop is clocked;

and a sequence counter connected to receive said output of said divide-by-n counter on a clock input and said output pulses from said pulse generator on a reset input, whereby said sequence counter produces a signal indicating when a double wide Manchester pulse has occurred, said signal being connected to reset said sampling flip-flop.

ABSTRACT OF THE DISCLOSURE

According to a broad aspect of the invention, an apparatus (34) for decoding a Manchester encoded data stream is provided. The apparatus includes a transition detector (45) for receiving the Manchester encoded data stream to produce a transition indicating output when a transition of the Manchester encoded data stream is detected. Also, a circuit (105) is provided to generate an output control pulse a predetermined time after the transition indicating output is produced. A sampling flip-flop (120) receives the Manchester encoded data stream, and is controlled by the output control pulse to output a state of the Manchester encoded data to an output control circuit (125) when the output control pulse is generated. In a preferred embodiment, the sampling flip-flop (125) operates to generate a binary NRZ form of the Manchester encoded data stream. The transition detector (45) may be configured to synchronize the transition indicating output with a pulse of a clock pulse stream, and also may include a phase selector to select either the first or second symbol of the Manchester data to the output of the apparatus.

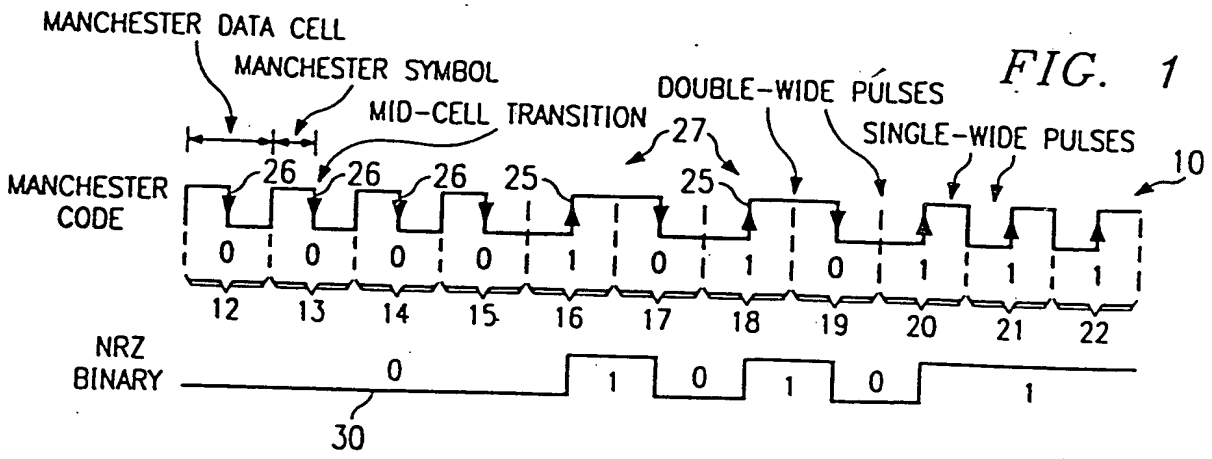


FIG. 1

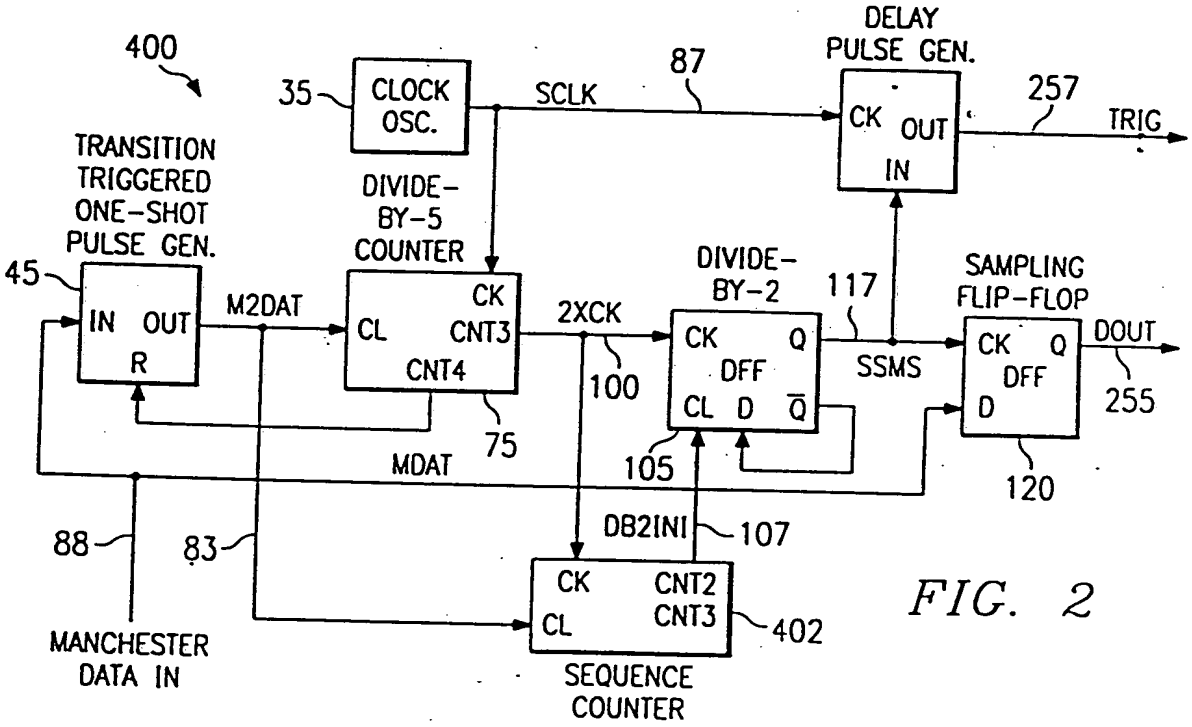


FIG. 2

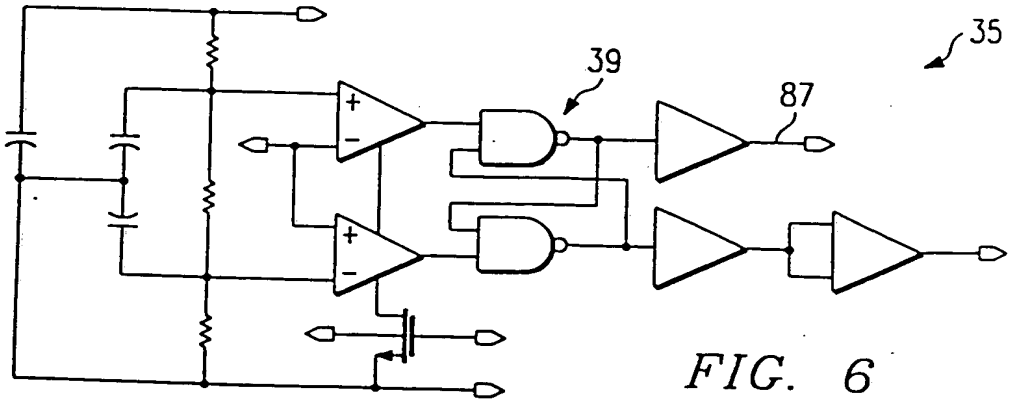


FIG. 6

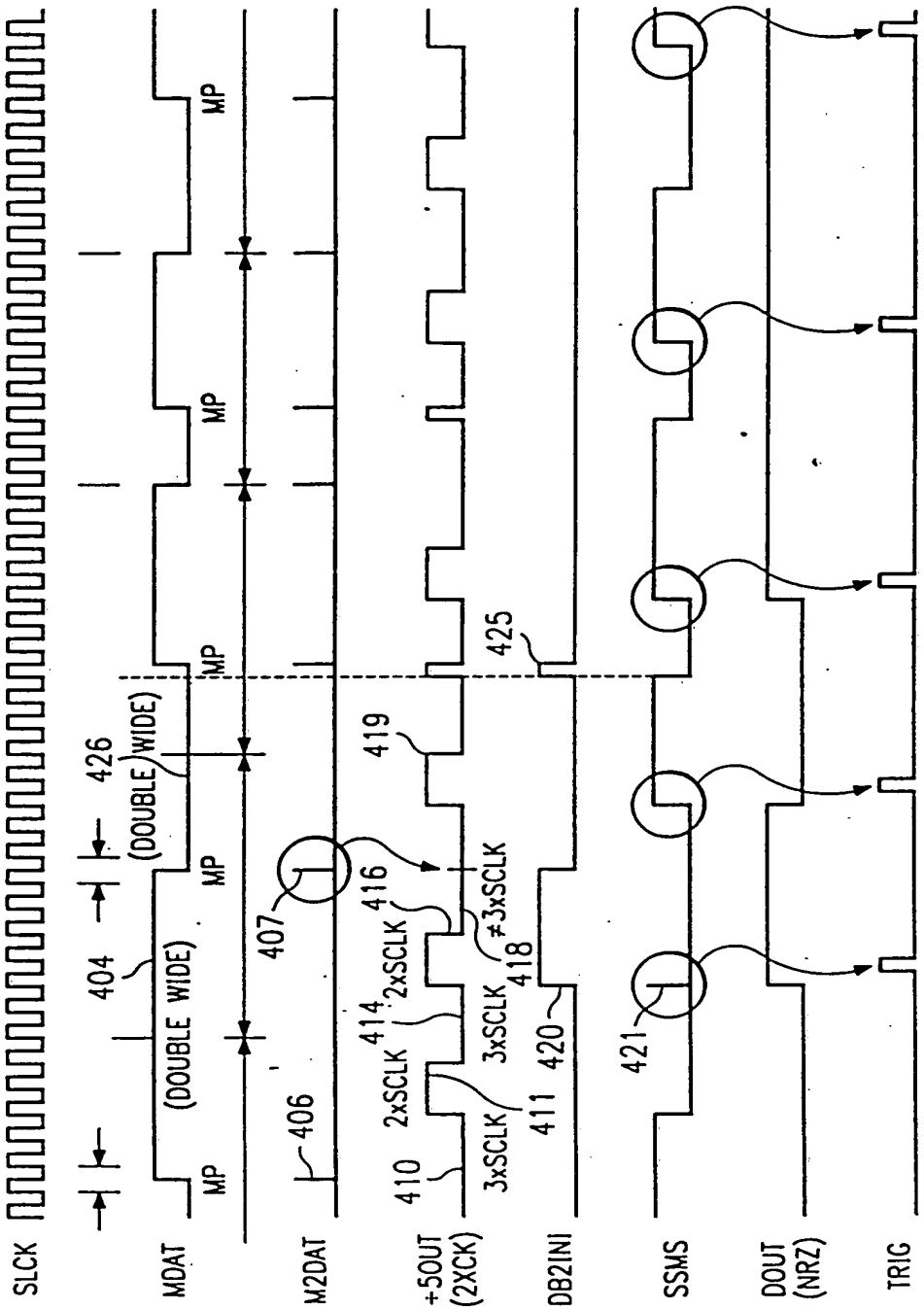
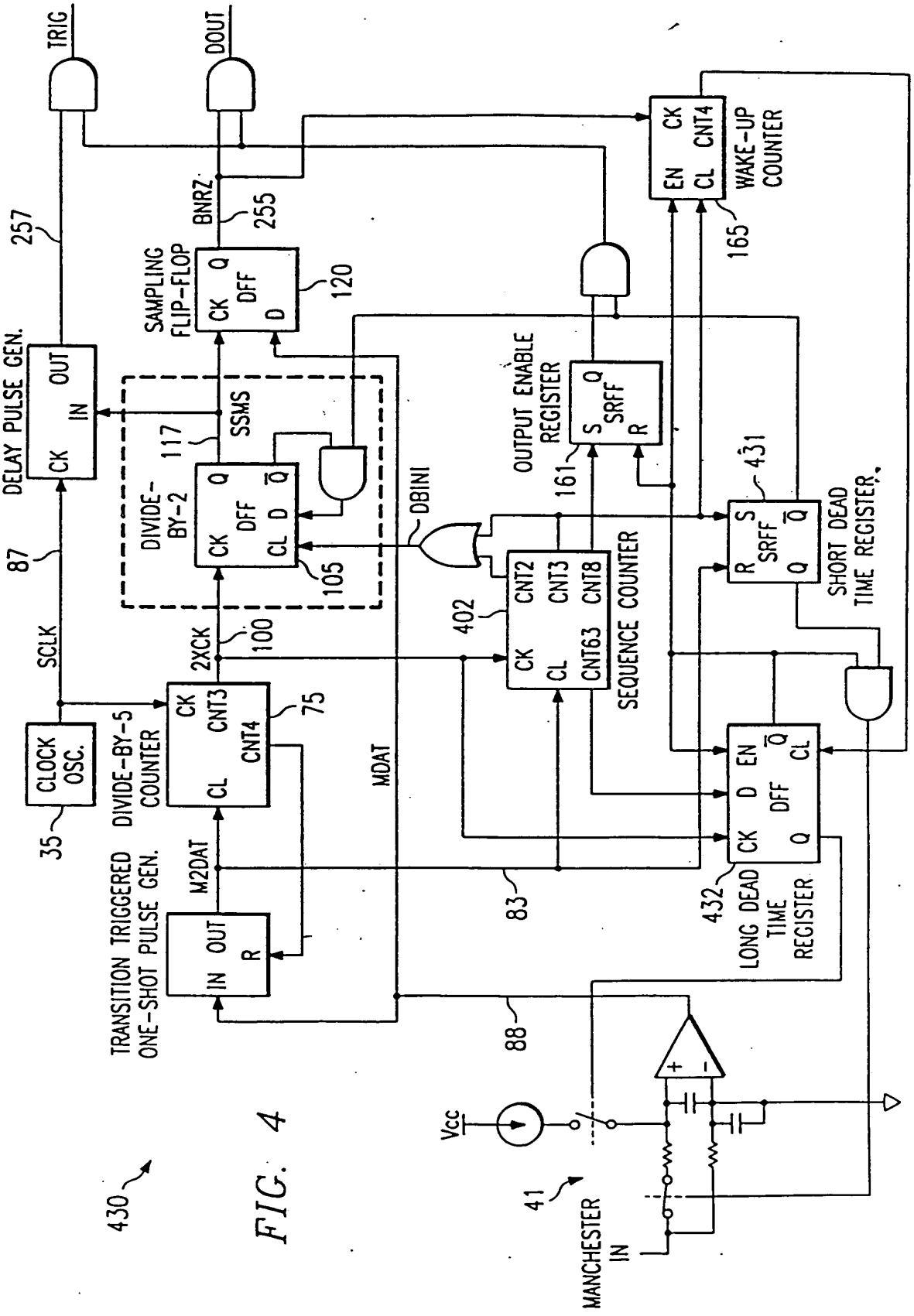

SLCK
MDAT
M2DAT
+5OUT (2XCK)
DB2INI
SSMS
DOUT (NRZ)
TRIG
MP
(DOUBLE WIDE)
404
426
(DOUBLE WIDE)
406
407
410
411
414
2xSCLK
3xSCLK
416
2xSCLK
3xSCLK
418
419
420
421
425

FIG. 3.


TRIG
DOUT
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BNRZ
255
SAMPLING FLIP-FLOP
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120
WAKE-UP COUNTER
EN CK CL CNT4
165
DELAY PULSE GEN.
CK IN OUT
87
SCLK
SSMS
117
DIVIDE-BY-2
CK Q DFF CL D Q
105
DBINI
OUTPUT ENABLE REGISTER
S SRFF R Q
161
431
SHORT DEAD TIME REGISTER
R S SRFF Q Q
2XCK
100
402
CNT2 CNT3 CNT8
CK CL CNT63
SEQUENCE COUNTER
CLOCK OSC.
35
DIVIDE-BY-5 COUNTER
CK CNT3 CNT4 CL
75
MDAT
M2DAT
TRANSITION TRIGGERED ONE-SHOT PULSE GEN.
IN OUT R
83
LONG DEAD TIME REGISTER
CK D EN DFF CL Q
432
88
Vcc
41
MANCHESTER IN
430

FIG. 4

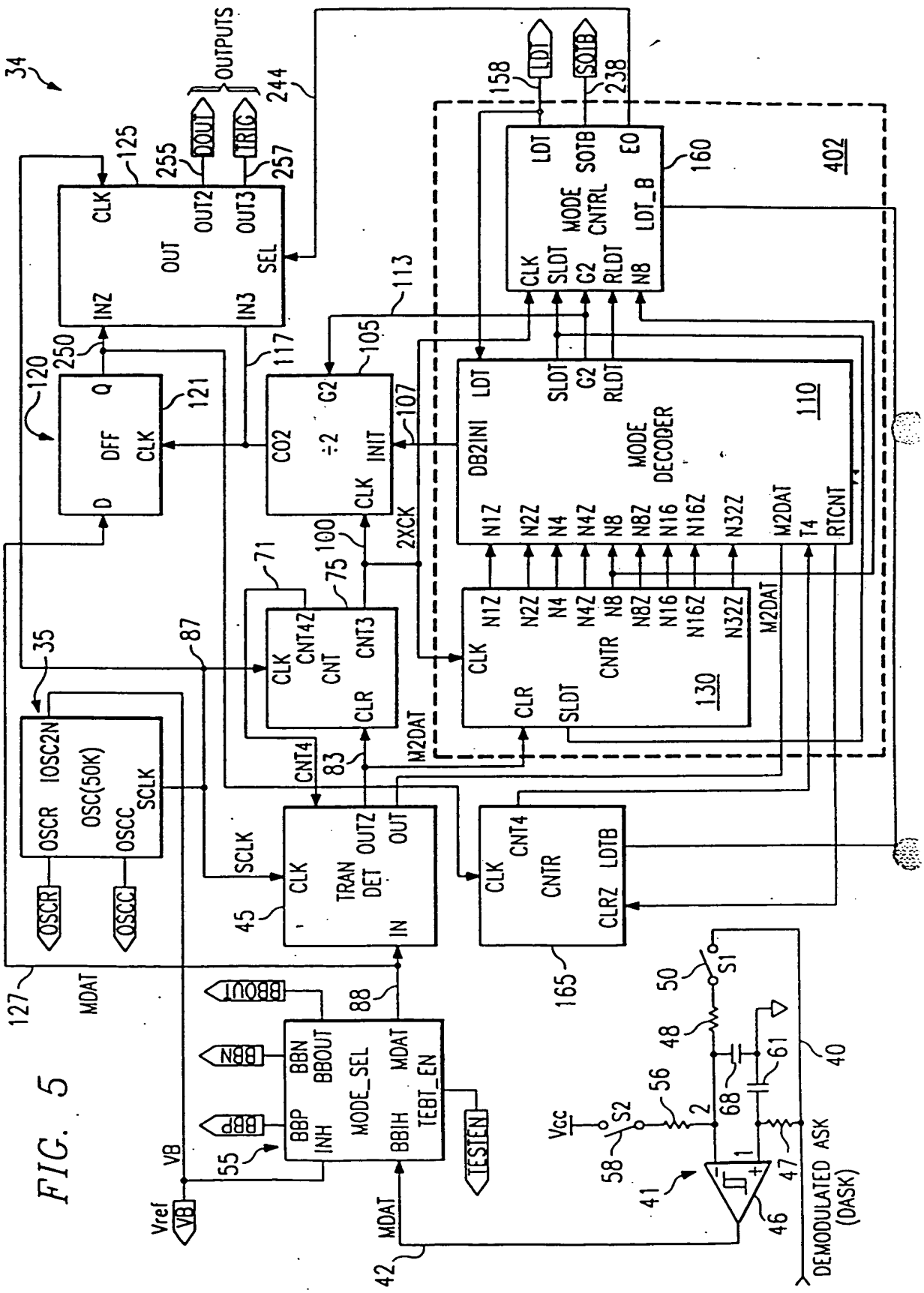
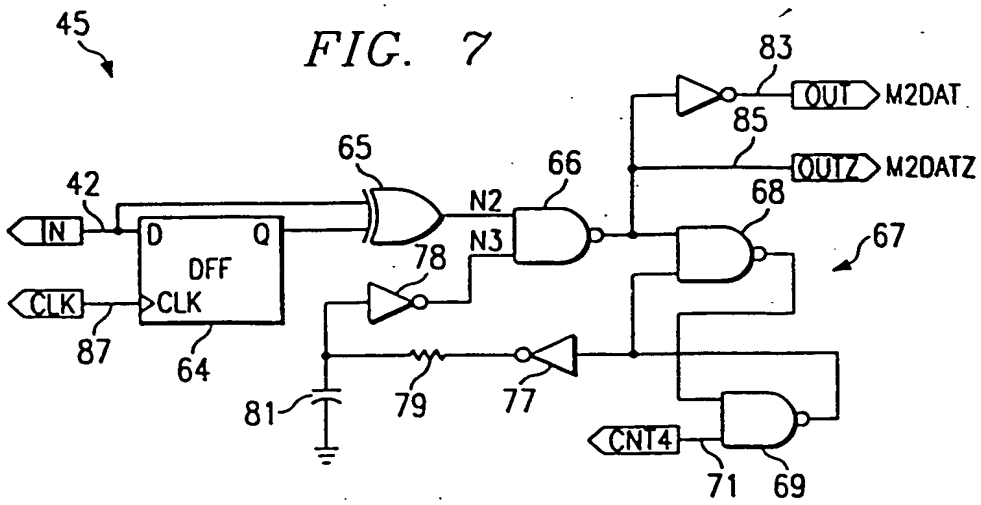

34
OUTPUTS
DOUT
TRIG
255
257
244
125
CLK
OUT
OUT2
OUT3
SEL
IN2
IN3
250
120
Q
DFF
CLK
D
121
117
105
G2
÷2
CO2
INIT
CLK
107
113
158
LDT
SOTB
238
LDT
SOTB
EO
MODE
CNTRL
LDT_B
160
402
CLK
SLDT
G2
RLDT
N8
DB2INI
LDT
SLDT
G2
RLDT
MODE
DECODER
110
N1Z
N2Z
N4
N4Z
N8
N8Z
N16
N16Z
N32Z
M2DAT
T4
RTCNT
100
2XCK
71
75
CNT4Z
CNT
CNT3
CLK
CLR
35
87
OSCR
IOSC2N
OSC(50K)
OSCC
SCLK
CNT4
83
M2DAT
CLR
SLDT
CNTR
130
OSCR
OSCC
SCLK
45
TRAN
DET
OUTZ
OUT
IN
CNT4
CNTR
CLRZ
LDTB
165
127
MDAT
BBOUT
88
BBN
BBOUT
BBP
INH
MODE_SEL
MDAT
BBIH
TEBT_EN
TESTEN
55
VB
Vref
VB
MDAT
42
Vcc
S2
58
56
2
1
41
S1
50
48
61
68
47
46
40
DEMODULATED ASK
(DASK)

FIG. 5

FIG. 7



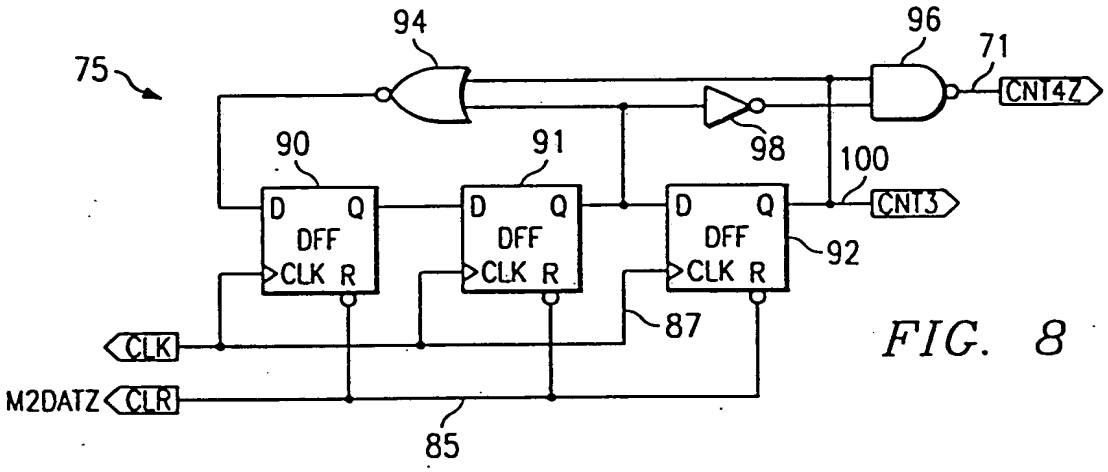


FIG. 8

FIG. 9

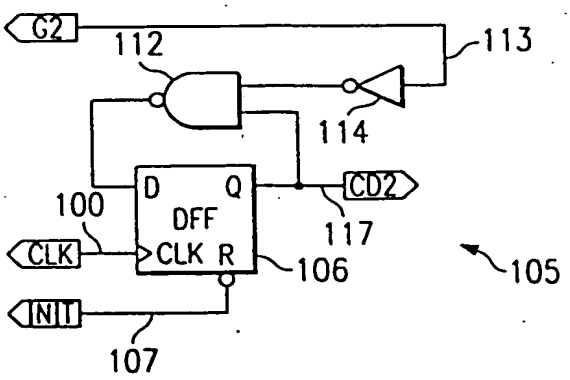
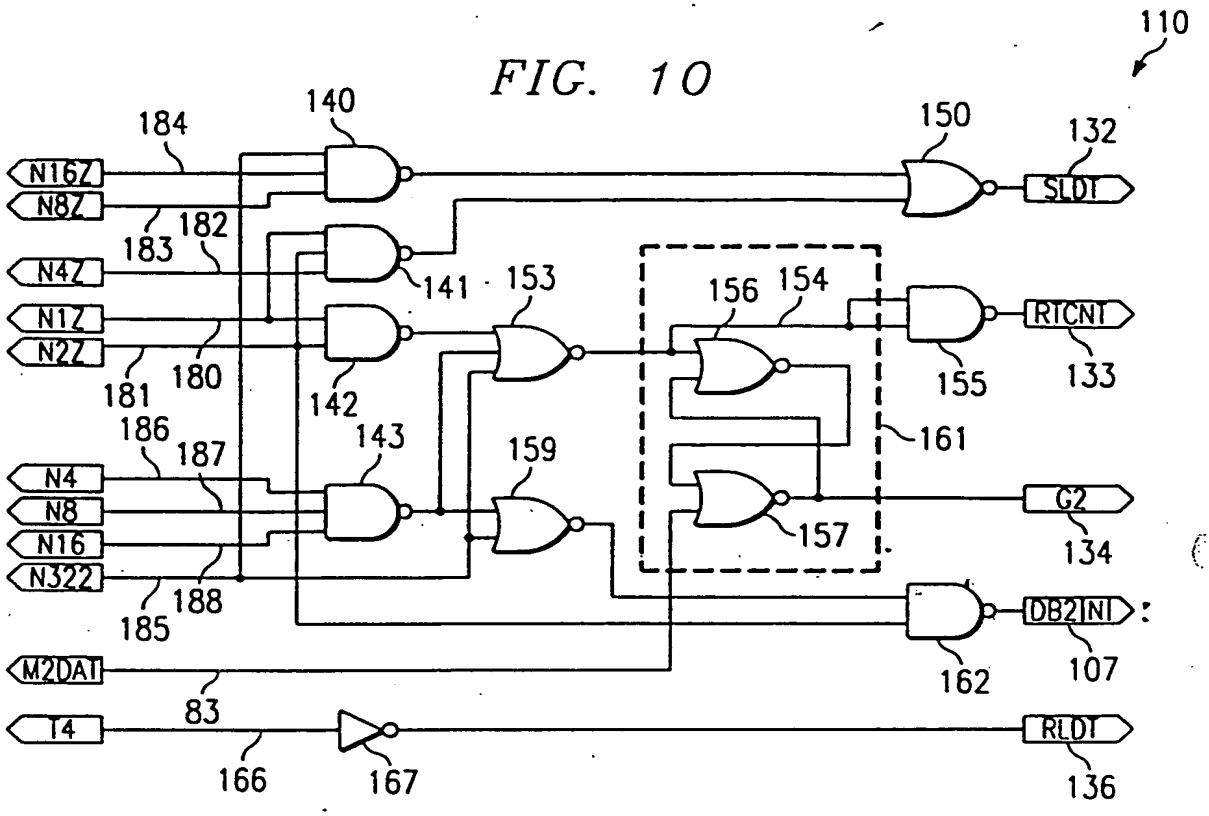


FIG. 10


110
140
184
150
132
N16Z
N8Z
SLDI
183
182
N4Z
141
153
156
154
N1Z
N2Z
RTCNT
181
180
142
155
133
186
187
143
159
161
N4
N8
N16
N322
157
G2
134
188
185
DB2INI
107
M2DAT
162
83
T4
RLDI
166
167
136

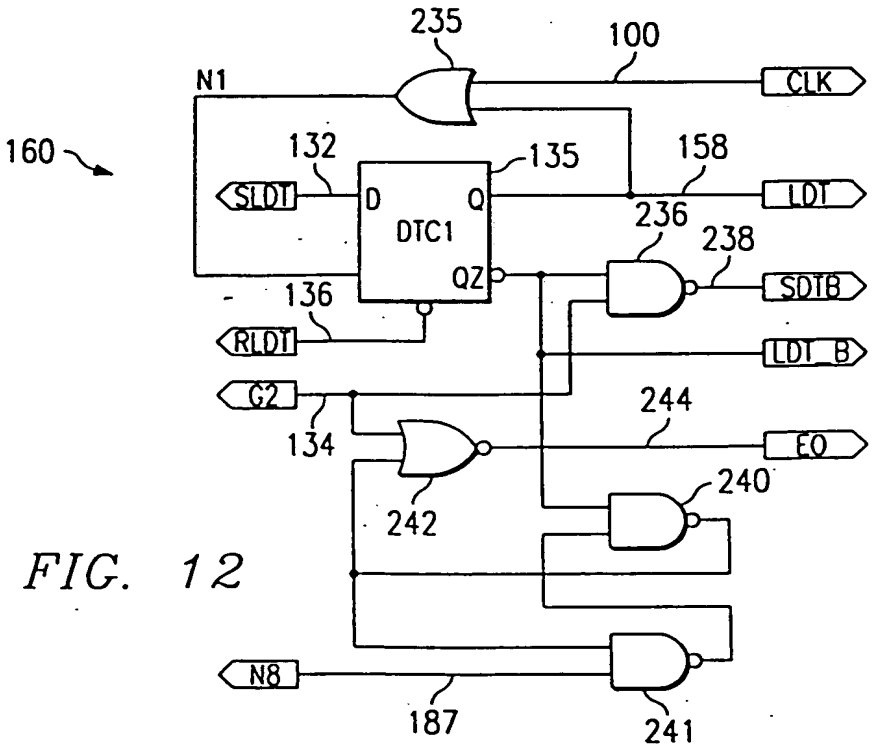

160
235
100
N1
CLK
132
135
158
SLDI
D
Q
LDI
DTC1
236
238
QZ
SDTB
136
RLDT
LDI_B
G2
244
134
EO
240
242
N8
187
241

FIG. 12

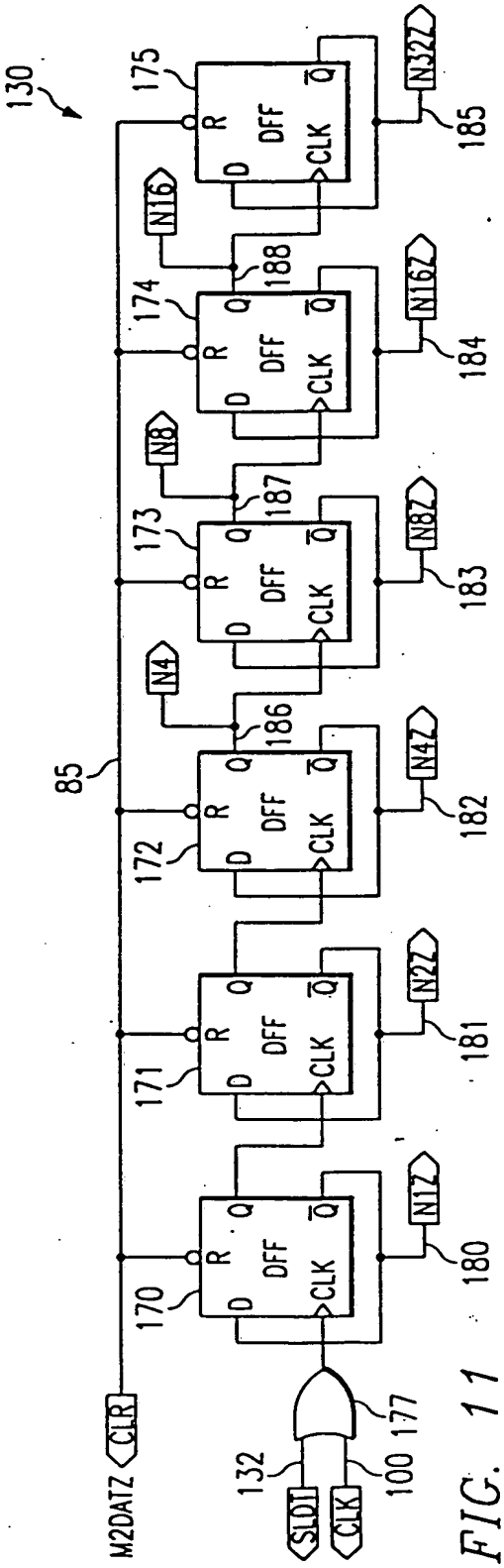

130
175
N32Z
185
N16
188
174
N16Z
184
N8
187
173
N8Z
183
N4
186
172
N4Z
182
85
171
N2Z
181
170
N1Z
180
M2DATZ
CLR
132
177
100
SLOT
CLK
D
R
Q
DFF
CLK

FIG. 11

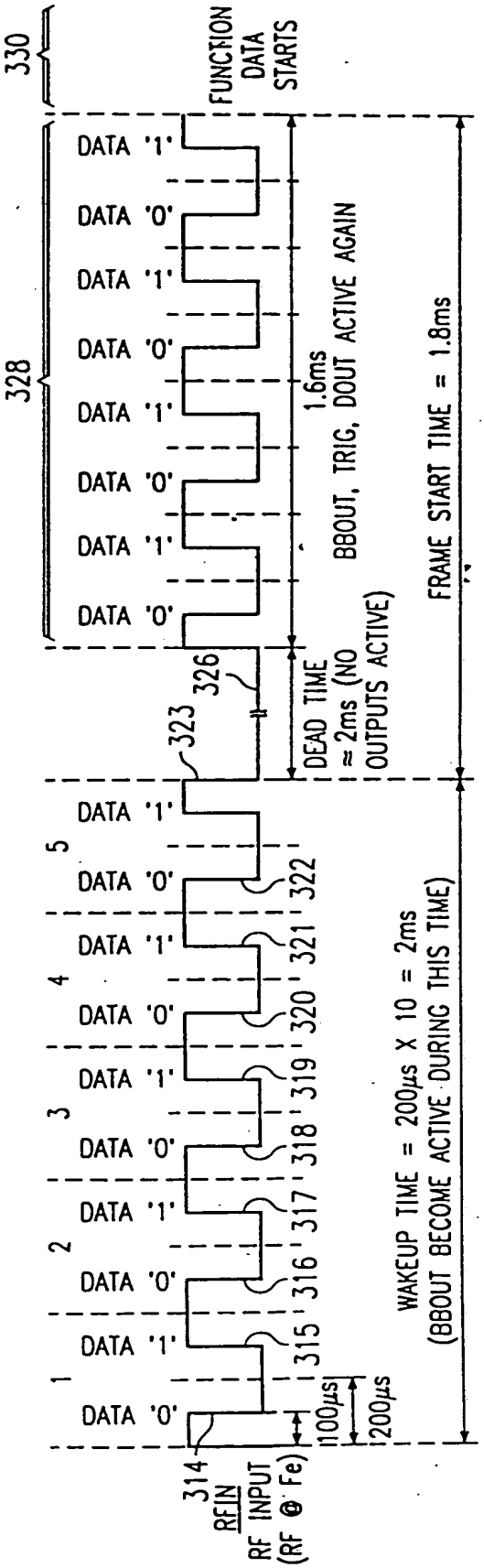

330
328
FUNCTION DATA STARTS
DATA '1'
DATA '0'
DATA '1'
DATA '0'
DATA '1'
DATA '0'
DATA '1'
DATA '0'
1.6ms
BBOUT, TRIG, DOUT ACTIVE AGAIN
323
326
DEAD TIME
≈ 2ms (NO OUTPUTS ACTIVE)
FRAME START TIME = 1.8ms
5
4
3
2
1
DATA '1'
DATA '0'
DATA '1'
DATA '0'
DATA '1'
DATA '0'
DATA '1'
DATA '0'
DATA '1'
DATA '0'
322
321
320
319
318
317
316
315
314
WAKEUP TIME = 200μs X 10 = 2ms
(BBOUT BECOME ACTIVE DURING THIS TIME)
100μs
200μs
RFIN
RF INPUT
(RF @ Fe)

FIG. 17

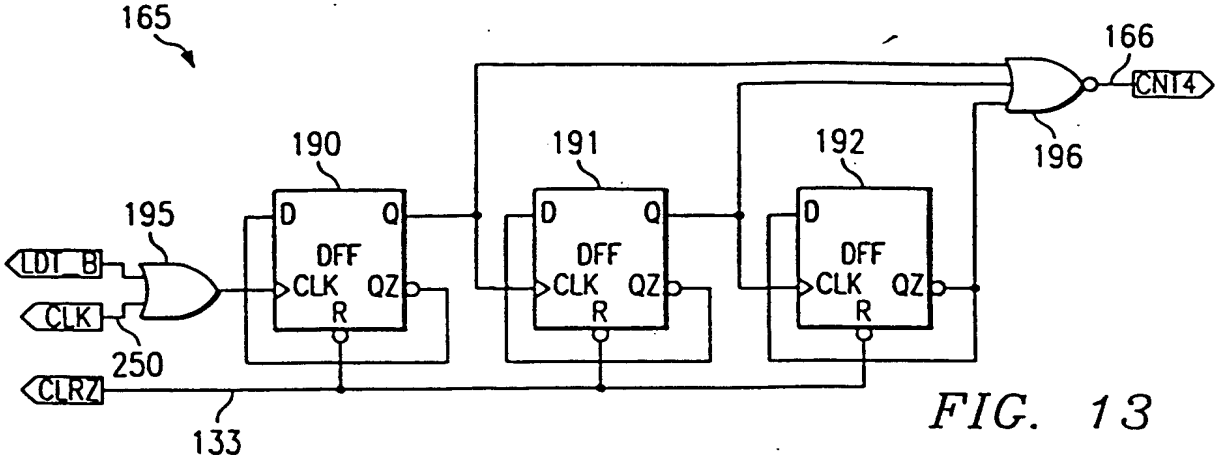


FIG. 13

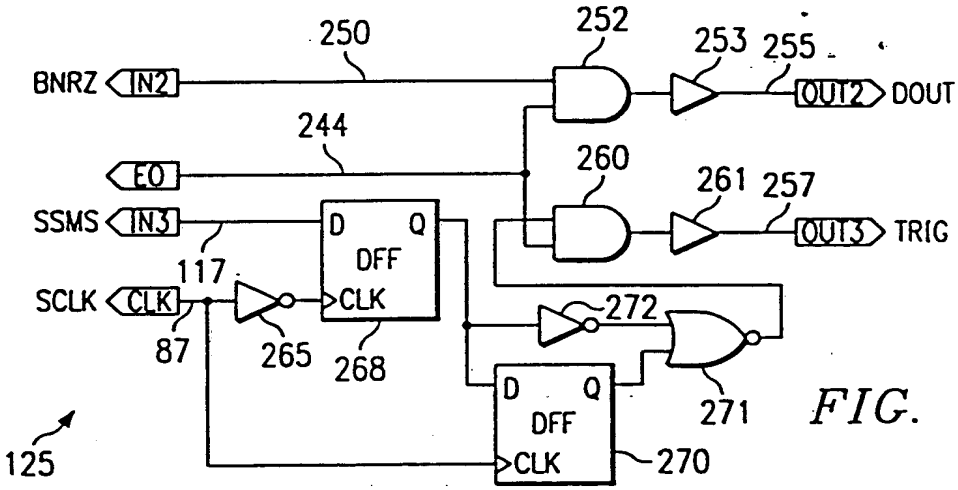


FIG. 14

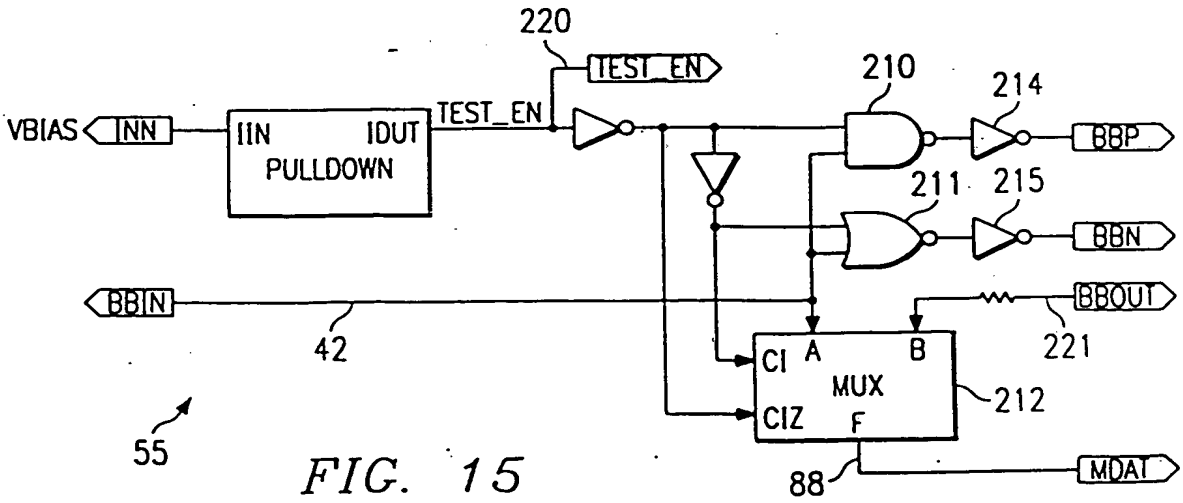


FIG. 15

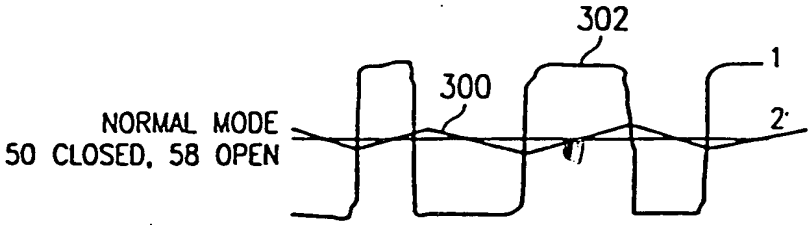


FIG. 16A

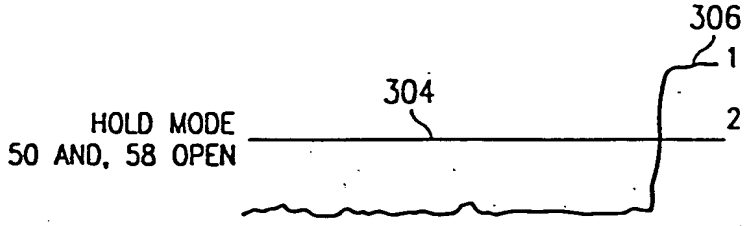


FIG. 16B

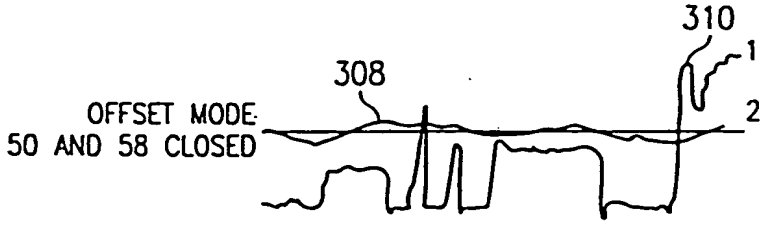


FIG. 16C

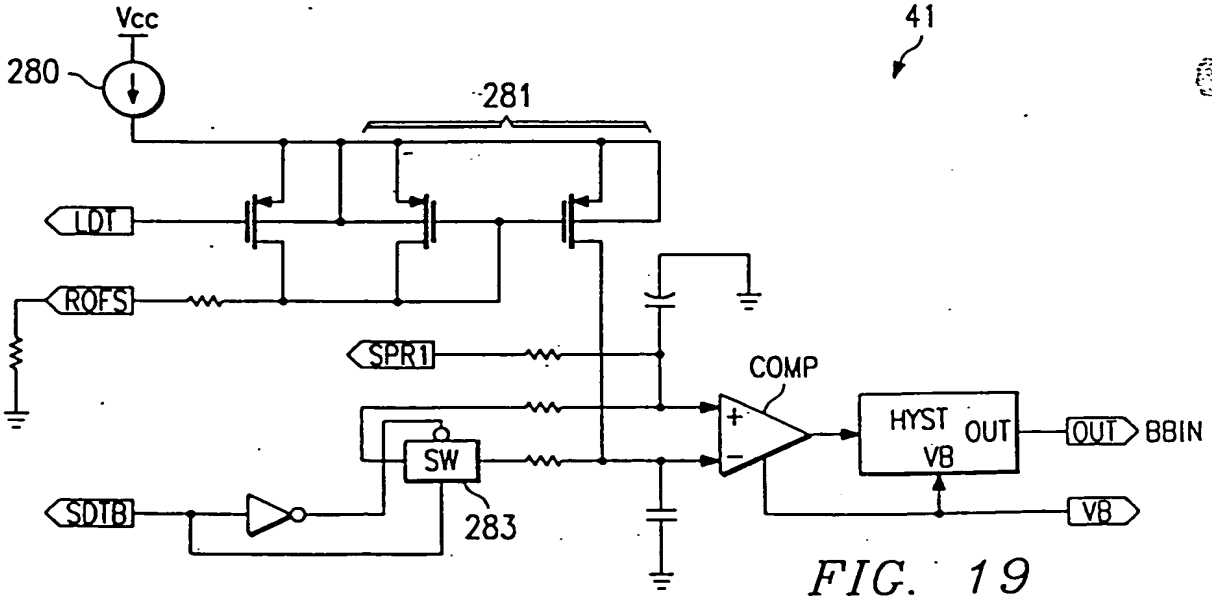


FIG. 19

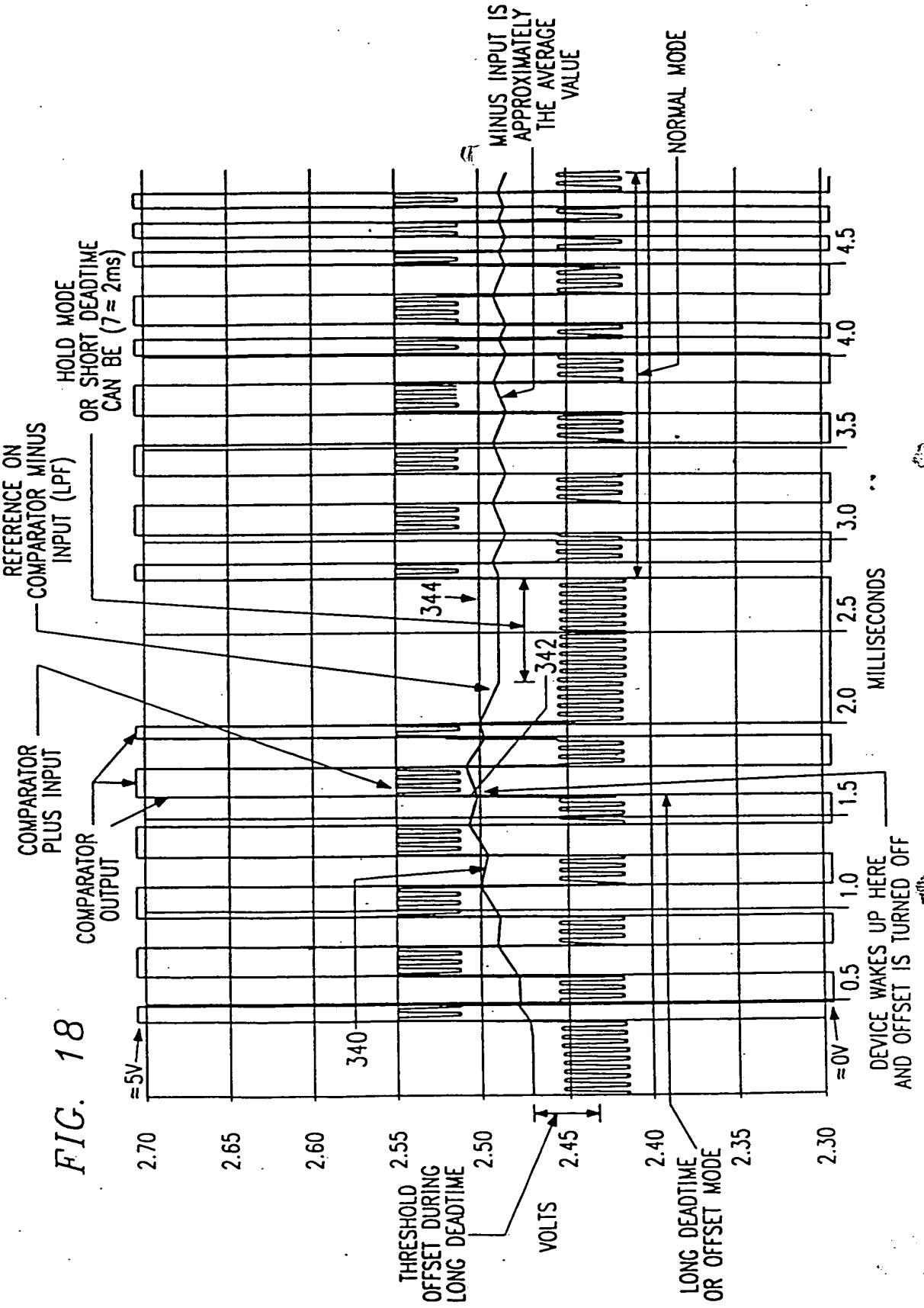

REFERENCE ON COMPARATOR MINUS INPUT (LPF)
HOLD MODE OR SHORT DEADTIME CAN BE (7≈ 2ms)
MINUS INPUT IS APPROXIMATELY THE AVERAGE VALUE
NORMAL MODE
COMPARATOR PLUS INPUT
COMPARATOR OUTPUT
344
342
340
≈5V
≈0V
2.70
2.65
2.60
2.55
2.50
2.45
2.40
2.35
2.30
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
MILLISECONDS
DEVICE WAKES UP HERE AND OFFSET IS TURNED OFF
THRESHOLD OFFSET DURING LONG DEADTIME
VOLTS
LONG DEADTIME OR OFFSET MODE

FIG. 18